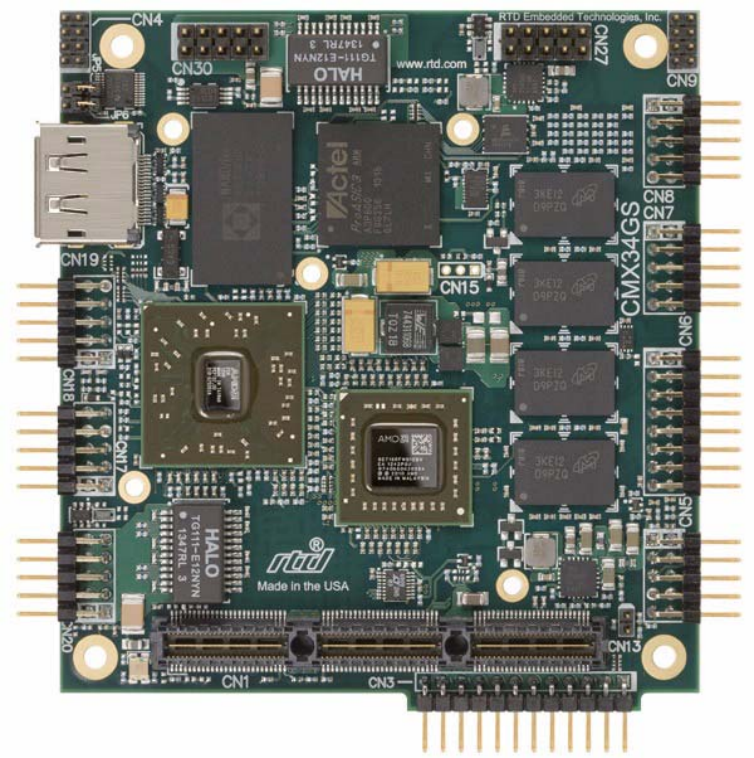
CMX34GS cpuModules™



User's Manual

BDM-610000082 Revision A

www.rtd.com

ISO9001 and AS9100 Certified

"Accessing the Analog World"®

CMX34GS cpuModules™ User's Manual

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Revision History

Revision	Date	Reason for Change
A	07/15/2014	Initial release

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Chapter 1 Introduction

This manual provides comprehensive hardware and software information for users developing with the CMX34GS PCIe/104 cpuModule.

Note *Read the specifications beginning on page 9 prior to designing with the cpuModule.*

This manual is organized as follows:

Chapter 1	***Introduction*** introduces main features and specifications
Chapter 2	***Getting Started*** provides abbreviated instructions to get started quickly
Chapter 3	***Connecting the cpuModule*** provides information on connecting the cpuModule to peripherals
Chapter 4	***Using the cpuModule*** provides information to develop applications for the cpuModule, including general cpuModule information, detailed information on storing both applications and system functions, and using utility programs
Appendix A	***Hardware Reference*** lists jumper locations and settings, physical dimensions, and processor thermal management
Appendix B	***Troubleshooting*** offers advice on debugging problems with your system
Appendix C	***IDAN™ Dimensions and Pinout*** provides connector pinouts for the cpuModule installed in an RTD Intelligent Data Acquisition Node (IDAN) frame
Appendix D	***Additional Information*** lists sources and websites to support the cpuModule installation and configuration
Appendix E	***Limited Warranty***

CMX34GS cpuModules

RTD's CMX34GS cpuModule represents the latest in low power PCI Express embedded controllers. Based on an AMD Fusion G-Series APU processor and chipset, the CMX34GS is offered with either a low power 615 MHz Single-Core processor or a high performance 1.0 GHz Dual-Core processor that supports a 1.33 GHz frequency on one core, complete with a DDR3 memory interface operating at up to 800 MT/s (400 MHz). All memory chips are soldered directly onto the board.

The video interface of the cpuModule's G-Series APU processor is an internal AMD Radeon HD 6250 (615 MHz single core option) running up to 276 MHz or the HD 6290 (1 GHz dual core option) which runs up to 400 MHz. Both options provide dual analog SVGAand DisplayPort outputs. The two video outputs are independent, and can display separate images and display timings, with audio support on the DisplayPort. Maximum resolution of both video outputs is 1920 x 1200.

A Serial-ATA (SATA) controller provides a fast 3.0 Gbit/sec connection to the hard drives. Network connectivity is provided by two integrated 10/100/1000 Mbps Ethernet controllers. High-speed peripheral connections include USB 2.0, with up to 480 Mb/sec data throughput. Four additional SATA links and USB 2.0 connections permit further expandability on the top and bottom-side PCIe/104 Type 2 connectors, along with x1 PCI Express Gen 2.0 links. Other features include two RS-232/422/485 COM ports and Advanced Digital I/O (aDIO).

RTD has gone the extra mile to include additional advanced features for maximum flexibility. These include an onboard SATA surface-mount flash drive with a standard SATA interface. An Advanced Watchdog Timer is provided that can generate an interrupt or reset when the timer expires. The CMX34GS is also available in a rugged, fanless IDAN enclosure.

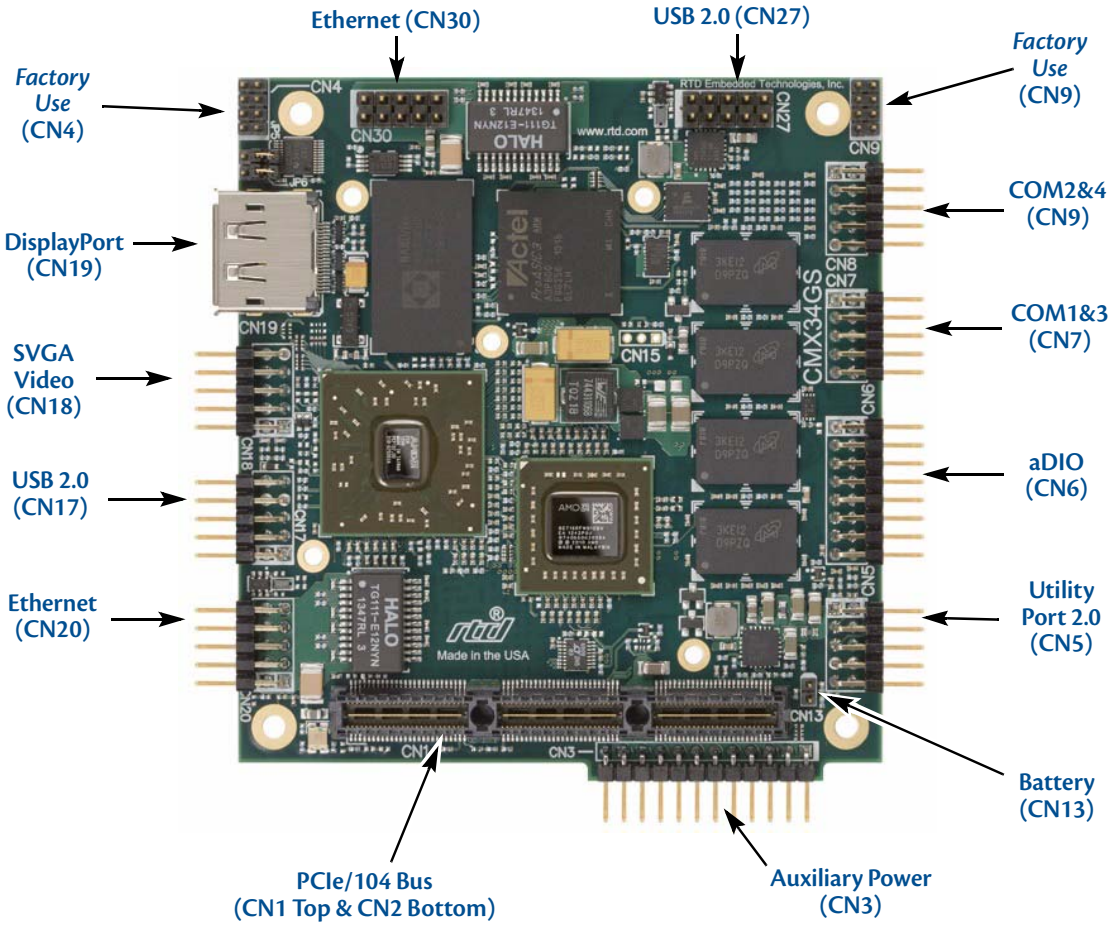

Figure 1 CMX34GS cpuModule (top view)

You can easily customize the cpuModule by stacking PCI/104-Express or PCIe/104 modules such as video controllers, Digital Signal Processors, drive carriers, LAN controllers, or analog and digital data acquisition modules. Stacking modules onto the cpuModule avoids expensive installations of backplanes and card cages, and preserves the module's compactness.

The cpuModule uses the RTD Enhanced BIOS. Drivers in the BIOS allow booting from hard disk,, or UEFI shell, thus enabling the system to be used with traditional disk drives or nonmechanical drives. Boot from USB devices and network are also supported.

The cpuModule and BIOS are also compatible with any real-time operating systems for PC compatible computers, although these may require creation of custom drivers to use the aDIO and watchdog timer.

aDIO

RTD's exclusive aDIO™ is 12 digital bits configured as 8 bit-direction programmable and 4-bit port-direction programmable I/O, plus 2 strobe inputs giving you any combination of inputs and outputs. Match, event, and strobe interrupt modes mean no more wasting valuable processor time polling digital inputs. Interrupts are generated when the 8 bit-direction programmable digital inputs match a pattern or on any value change event. Bit masking allows selecting any subgroup of eight bits. The strobe input latches data into the bit-programmable port and generates an interrupt.

Ordering Information

The CMX34GS cpuModule is available with a selection of processors and memory sizes. The cpuModule can also be purchased as part of an Intelligent Data Acquisition Node (IDAN™) building block, which consists of the cpuModule and a milled aluminum IDAN frame. The IDAN building block can be used in just about any combination with other IDAN building blocks to create a simple but rugged PC/104 stack. Refer to Appendix C, *IDAN™ Dimensions and Pinout*, for more information. The CMX34GS cpuModule can also be purchased as part of a custom-built RTD HiDAN™ or HiDAN*plus* High Reliability Intelligent Data Acquisition Node. Contact RTD for more information on its high reliability PC/104 systems.

CMX34GS Model Options

The basic cpuModule model options are shown below. Refer to the RTD website (www.rtd.com) for more detailed ordering information and any new variations that may be available.

Table 1 CMX34GS cpuModule Model Options

Part Number	Description
CMX34GSS615HR-2048	AMD G-Series, Single Core 615 MHz, 2GB DDR3-SDRAM
CMX34GSD1000HR-2048	AMD G-Series, Dual Core 1 GHz, 2GB DDR3-SDRAM

Cable Kits and Accessories

For maximum flexibility, RTD does not provide cables with the cpuModule. You may wish to purchase the CMX34GS cpuModule cable kit (P/N XK-CM109), which contains:

- Utility Port 2.0 multi-function cable (2x USB 2.0 ports, battery, reset button, power button, speaker)
- Two serial port cables (DIL-10 to DSUB-9)
- VGA monitor cable (DIL-10 to high density 15-pin DSUB)
- aDIO cable (DIL-16 to DSUB-25)
- Four USB cables (5-pin SIL to USB A)
- PCIe/104 Type 2 break-out board (provides standard PC interfaces for SATA and USB devices)
- Two Ethernet cables (DIL-10 to RJ-45)

For additional accessories, refer to the RTD website.

Board Features

- AMD Fusion G-Series FT1 Processor:

Part Number	Cores	Core Frequency	Boost Frequency	L1 Cache (data)	L1 Cache (instruction)	L2 Cache
CMX34GSS615	One	615 MHz	—	32 KByte	32 KByte	512 KByte
CMX34GSD1000	Two	1.0 GHz	1333 MHz[1]	32 KByte[2]	32 KByte[2]	512 KByte[2]

1. For CPU boost, only one processor of the dual-core will have boost enabled
2. Discreet L1 and L2 cache structures for each core

  - AMD64 technology
  - ACPI-compliant, including support for processor performance (P-states) and sleep states including S0, S3, S4, and S5
  - Thermal Throttling reduces clock speed to prevent thermal runaway (dual-core only)
  - Supports AMD Virtualization™ technology
  - 40 nm process
- AMD G-Series A55E Platform Controller Hub
- 2GBytes BGA DDR3 SDRAM
  - Single-channel memory interface
  - 800 MT/s (400MHz) Data Rate
  - Surface Mounted for maximum reliability
- Stackable 156-pin PCIe/104 Type 2 bus on top
  - x1 PCI Express Gen 2.0 Links (up to 5.0 GT/s per lane)
  - Two SATA 2.0
  - Two USB 2.0
- Stackable 156-pin PCIe/104 Type 2 bus on bottom
  - Four PCI Express x1 Links
  - Two SATA 2.0
  - Two USB 2.0
- Advanced Thermal Management
  - Thermal Monitor throttles processor and memory to prevent thermal runaway
  - Passive Heastink
  - Passive Structural Heatsink & Heatpipes in IDAN and HiDAN System Configurations
- Advanced Programmable Interrupt Controller (APIC)
  - 24 interrupt channels with APIC enabled (15 in legacy PIC mode)
  - High Precision Event Timer
- Advanced Configuration and Power Interface (ACPI)
  - ACPI 3.0 Compliant
  - Supported power down modes: S3 (Suspend to RAM), S4 (Hibernate), and S5 (Soft-Off)
  - Wake events include:
    - USB event (device insertion, keyboard keystroke, etc.)
    - Real Time Clock alarm or timeout

    - Power Switch
    - etc.
- Real-Time Clock (external battery required to maintain time only)
- Nonvolatile storage of CMOS settings without battery
- Advanced Watchdog timer
- Complete PC-compatible Single Board Computer

I/O

- AMD Radeon Graphics

Part Number	Cores	Core Frequency	AMD Radeon	Graphics Clock Frequency (maximum)
CMX34GSS615	One	615 MHz	HD 6250	276 MHz
CMX34GSD1000	Two	1.0 GHz	HD 6290	400 MHz

- Analog VGA Interface
    - RGB CRT output
    - Maximum Resolution 1920 x 1200
- DisplayPort Interface
    - Supports all mandatory features of the VESA DisplayPort Standard (Version 1.1a)
    - Supports Dual-mode DisplayPort (DP++)
        - Can outupt single-link HDMI and DVI signals using a simple passive adapter
    - Maximum Resolution 1920 x 1200
    - Audio over DisplayPort supports up to 8 channels
- Dual Gigabit Ethernet
    - Two Intel 82574IT Controllers (PRO1000 Series)
    - 10/100/1000 Auto-negotiation
    - Jumbo Frame Support (9kB)
    - PXE network Boot
    - Automatic MDI/MDI-X crossover capable
- Software-configurable RS-232/422/485 serial ports
    - 16550 compatible UARTs for high-speed
    - 120 Ohm Termination resistors for RS-422/485 through BIOS Configuration
    - Each serial port connector can be configured as two limited serial ports, for a total of four serial ports
    - Fully jumperless configuration
- Advanced Digital I/O (aDIO)
    - One 8-bit bit-programmable I/O with Advanced Digital Interrupt Modes
    - One 4-bit port programmable as input or output
    - Event Mode Interrupt generates an interrupt when any input bit changes
    - Match Mode Interrupt generates an interrupt when input bits match a preset value
    - External Strobe Mode latches 8 data inputs and generates and interrupt

  - Two Strobes can be configured as readable inputs
- Four USB 2.0 (Universal Serial Bus) Ports
  - Supports 480 Mb/s (high-speed), 12Mb/s (full-speed), and 1.5Mbs (low speed) peripherals
  - Automatic resettable over-current protection (500 mA @ 5 Vdc per port)
  - USB Boot capability
- Serial ATA (SATA)
  - SATA revision 2.0 with transfer rates up to 3.0 Gbit/sec
  - Compatability mode supports legacy operating systems.
- Utility Port 2.0 Connector
  - 1x USB 2.0 (Univseral Serial Bus) Port
  - Speaker port (0.1W output)
  - Hardware Reset input
  - Soft Power Button input
  - Battery input for Real Time Clock
- Power I/O

RTD Enhanced BIOS

- User-configurable using built-in Setup program
- Flash-based CMOS Setup - No battery required to store CMOS settings
- Supports boot from SATA, USB, or Ethernet (PXE)
- UEFI (Unified Extensible Firmware Interface) Shell
- Special RTD Reliability Enhancements

Block Diagram

The next figure shows a simplified block diagram of the CMX34GS cpuModule.

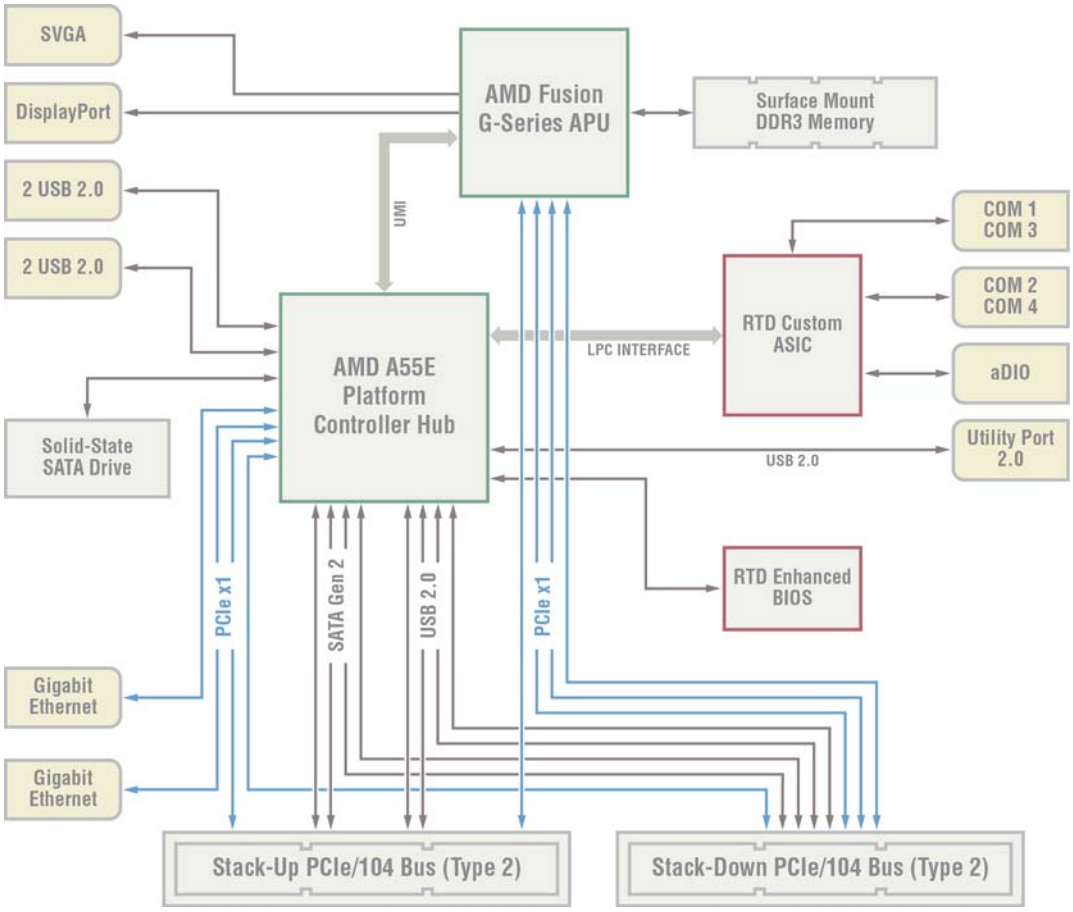

Figure 2 CMX34GS cpuModule Simplified Block Diagram

Specifications

Physical Characteristics

- Dimensions: 95.885mm L x 90.170mm W x 15.240mm H (3.775"L x 3.550"W x 0.600"H)
- Weight: Approximately 0.18 Kg (0.4 lb.) with Heatsink

Power Consumption

Exact power consumption depends on the actual application. Typical power consumption of the CMX34GS is listed in Table 2. Tables 3 and 4 list power consumption for common applications. It is expected that power consumption of a typical application will be a combination of these scenarios.

Table 2 Typical Power Consumption

Part Number	Typical Power Consumption
CMX34GSS615HR-2048	7.6 W
CMX34GSD1000HR-2048	9.1 W

Table 3 Power Consumption (615 MHz, Single Core)

	Idle	Single-Threaded Application	Multi-Threaded Application	CPU & Graphics Intensive Application	ACPI S3	ACPI S4/S5
+5 V Current Draw	1.2 A	1.3 A	—	1.3 A	0.2 A[1]	0.2 A[1]
+12 V Current Draw	0.1 A	0.1 A	—	0.2 A	—	—
Power Consumption	6.6 W	7.6 W	—	8.5 W	1.1 W	1.0 W

1. Current draw will be the same whether power is supplied to +5 V or +5V_STBY in S3 or S4/S5

Table 4 Power Consumption (1.0 GHz, Dual Core)

	Idle	Single-Threaded Application	Multi-Threaded Application	CPU & Graphics Intensive Application	ACPI S3	ACPI S4/S5
+5 V Current Draw	1.1 A	1.1 A	1.2 A	1.3 A	0.2 A[1]	0.2 A[1]
+12 V Current Draw	0.1 A	0.2 A	0.4 A	0.4 A	—	—
Power Consumption	6.1 W	8.6 W	10.7 W	11.1 W	1.0 W	0.9 W

1. Current draw will be the same whether power is supplied to +5 V or +5V_STBY in S3 or S4/S5

Note *The measurements listed above are intended to represent common usage scenarios. The cpuModule's power consumption is heavily influenced by the running software and system activity.*

Operating Conditions

Table 5 Operating Conditions

Symbol	Parameter	Test Condition	Min.	Max.
V_{CC5}	5V Supply Voltage		4.75V	5.25V
V_{CC12}	12V Supply Voltage		11.4V	12.6V
V_{CCSTBY}	5V Standby Voltage[1]		4.75V	5.25V
I_{CCSTBY}	5V Standby Current[1]		-	500mA
Ta	Ambient Operating Temperature[2]	Board IDAN	-40 -40	+70C +80C
Ts	Storage Temperature		-40	+60C
Rh	Humidity	Non-Condensing	0	90%

1. 5V Standby is used to power the board when the main supply is turned off (power down modes S3-S5). It is not required for board operation.
2. With supplied heat sink solution. Depending on the CPU usage, performance may degrade as the ambient temperature approaches the maximum. Contact RTD Tech Support for more information.

Electrical Characteristics

The table below lists the Electrical Characteristics of the CMX34GS. Operating outside of these parameters may cause permanent damage to the cpuModule.

Table 6 Electrical Characteristics

Symbol	Parameter	Test Condition	Min.	Max.
		USB Ports		
Ioc	Overcurrent Limit	Each port	0.5 A	5.0 A
		SVGA Port		
V_{OH}	Output Voltage High HSYNC, VSYNC	I_{OH} = −8.0 mA	2.4 V	3.3 V
V_{OL}	Output Voltage Low HSYNC, VSYNC	I_{OL} = 8.0 mA	0.0 V	0.5 V
V_{OH}	Output Voltage High DDC_*	I_{OH} = −4.0 mA	2.4 V	3.3 V
V_{OL}	Output Voltage Low DDC_*	I_{OL} = 8.0 mA	0.0 V	0.4 V
V_{IH}	Input Voltage High DDC_*	—	2.0 V	5.5 V
V_{IL}	Input Voltage Low DDC_*	—	-0.3 V	0.8 V
I_{DDCvcc}	Supply Current for DDC Electronics	—		500 mA
		DisplayPort		
I_{VCC}	Supply Current	—		500 mA
		Serial Ports - RS-232		
V_{OH}	Output Voltage High	R_L = 3 k	5.0 V	7.0 V
V_{OL}	Output Voltage Low	R_L = 3 k	-7.0 V	-5.0 V
V_{IH}	Input Voltage High	—	2.0 V	15 V
V_{IL}	Input Voltage Low	—	-15 V	0.6 V
		Serial Ports - RS-422/485		
V_{OD1}	Differential Output	R_L = 100 Ohm	2.0 V	
V_{OD2}	Differential Output	R_L = 54 Ohm	1.5 V	
V_{OC}	Common Mode Output	R_L = 54 or 100 Ohm		3.0 V
V_{TH}	Differential Input Threshold		-200 mV	-50 mV
V_I	Absolute Max Input Voltage		-18 V	18 V
		aDIO		
V_{OH}	Output Voltage High	I_{OH} = −29 mA	2.4 V	3.3 V
V_{OL}	Output Voltage Low	I_{OL} = 17 mA	0.0 V	0.5 V
V_{IH}	Input Voltage High	—	1.8 V	5.5 V
V_{IL}	Input Voltage Low	—	-0.3 V	0.8 V
$I_{ADIOvcc}$	Supply current	—		500 mA

Table 6 Electrical Characteristics

Symbol	Parameter	Test Condition	Min.	Max.
T_{MIN}	Update Interval	—	1ms	
	Utility Port 2.0 Connector (CN5)			
V_{RTC}	Input RTC Voltage[1]	—	2.5V	3.6 V
I_{RTC}	RTC Battery Current	—		< 4 uA
$I_{UTILvcc}$	Utility Supply Current	—		500 mA

1. Only required to maintain date and time when power is completely removed from the system. Not required for board operation.

Migrating to RTD's G-Series cpuModules

When migrating to RTD's AMD G-Series cpuModules, there are several differences from preceding cpuModule product families of which the customer should be aware.

Connector Pinout & Function Differences

The newer AMD G-Series cpuModules have several connector-related differences, which are summarized below. Complete information about the connectors on the CMX34GS can be found in Chapter 3, *Connecting the cpuModule*.

New I/O Connectors

The CMX34GS cpuModule introduces a new I/O connector that was not present on previous RTD cpuModules:

- **DisplayPort (CN19)**
  - Provides video and audio output
  - Unlike legacy LVDS and flat panel connectors which needed to have their BIOS pre-configured to a specific manufacturer's flat panel parameters, the DisplayPort connector is compatible with any display that has a DisplayPort interface.

Connector Differences

While some connectors on the CMX34GS have identical pinouts as on previous cpuModule generations, the features of the connector are sometimes different. Other connectors have entirely different pinouts than those on previous cpuModule generations. Connectors with pinout and feature differences include:

- **Auxiliary Power Connector (CN3)**
  - 12 pins (unlike the 10-pin connector on RTD Montevina cpuModules)
  - +5V and +12V inputs (unlike +5V only auxilliary power connectors found on all previous RTD cpuModule generations)
  - The Auxilliary Power Connector excludes ATX power signaling. The ATX power signals are provided on the PCIe/104 Type 2 bus connectors.
- **Utility Port 2.0 (CN5)**
  - Replaces the legacy Utility Port multi-function connector
  - Replaces the PS/2 Mouse and Keyboard connections with one USB 2.0 port
  - The pinout of the Utility Port 2.0 is **not** compatible with previous generations of RTD cpuModules.
- **COM Ports (CN7 and CN8)**
  - Connector **CN7** can be configured to output Serial POST codes out of the TXD pin when in single RS-232 mode (unlike RTD Montevina cpuModules, where the DTR pin was configured for serial POST code output on the second port of CN7 in dual-port mode). For more information, refer to *Serial Power-On-Self-Test (POST) Code Output* on page 73.
  - Of all single and dual-port modes, only the single RS-232 pinout is compatible with previous generations of RTD cpuModules.
  - Dual-mode COM port pinouts permit dual RS-232, dual RS-422, and dual RS-485 modes. Unlike some previous generations of RTD cpuModules, a dual "combined" mode with RS-232 and RS-422/458 is not supported.
  - Unlike some previous cpuModule generations, the single-mode RS-422/485 pinouts of the CMX34GS do not include the DCD, DSR, DTR, and RI signals.

– When a COM port connector is configured for dual-port mode, enabling/disabling COM port termination enables/disables the termination for both ports on that connector. (Some previous generations of cpuModules have the ability to independently enable/disable termination on both ports when configured for dual-mode.)

Software Differences

The newer AMD G-Series cpuModules have several software-related differences, which are summarized below. Complete information about these CMX34GS features can be found in Chapter 4, *Using the cpuModule*.

aDIO

While the 16-pin aDIO connector is pin-for-pin compatible with previous generations of RTD cpuModules (such as the Montevina series), the hardware is slightly different, and requires that writes ands reads to/from the aDIO ports happen no more than once per millisecond. Migrating legacy software to the G-Series that utilizes RTD's Advanced Digital I/O may require that you add this delay prior to all reads and writes.

UEFI Shell

Previous generations of RTD cpuModules contained a Failsafe Boot ROM image, which permitted the cpuModule to boot to a DOS prompt even when no disk drives were connected to the system. The RTD G-Series cpuModules provide a similar prompt, called the Unified Extensible Firmware Interface (UEFI) Shell, which provides an enviroment to execute simple commands when no bootable devices are connected to the system.

Contact Information

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Chapter 2 Getting Started

For many users, the factory configuration of the CMX34GS cpuModule can be used to get a PC/104 system operational. You can get your system up and running quickly by following the simple steps described in this chapter, which are:

1. Before connecting the cpuModule, the user must be properly grounded to prevent electrostatic discharge (ESD). For more information, refer to *Proper Grounding Techniques* on page 26.
2. Connect power.
3. Connect the Utility Port 2.0 cable.
4. Connect a USB keyboard.
5. Default BIOS configuration.
6. UEFI (Unified Extensible Firmware Interface) shell.
7. Connect a monitor to the SVGA connector or DisplayPort interface.

Refer to the remainder of this chapter for details on each of these steps.

Connector Locations

Figure 3 shows the connectors of the CMX34GS cpuModule.

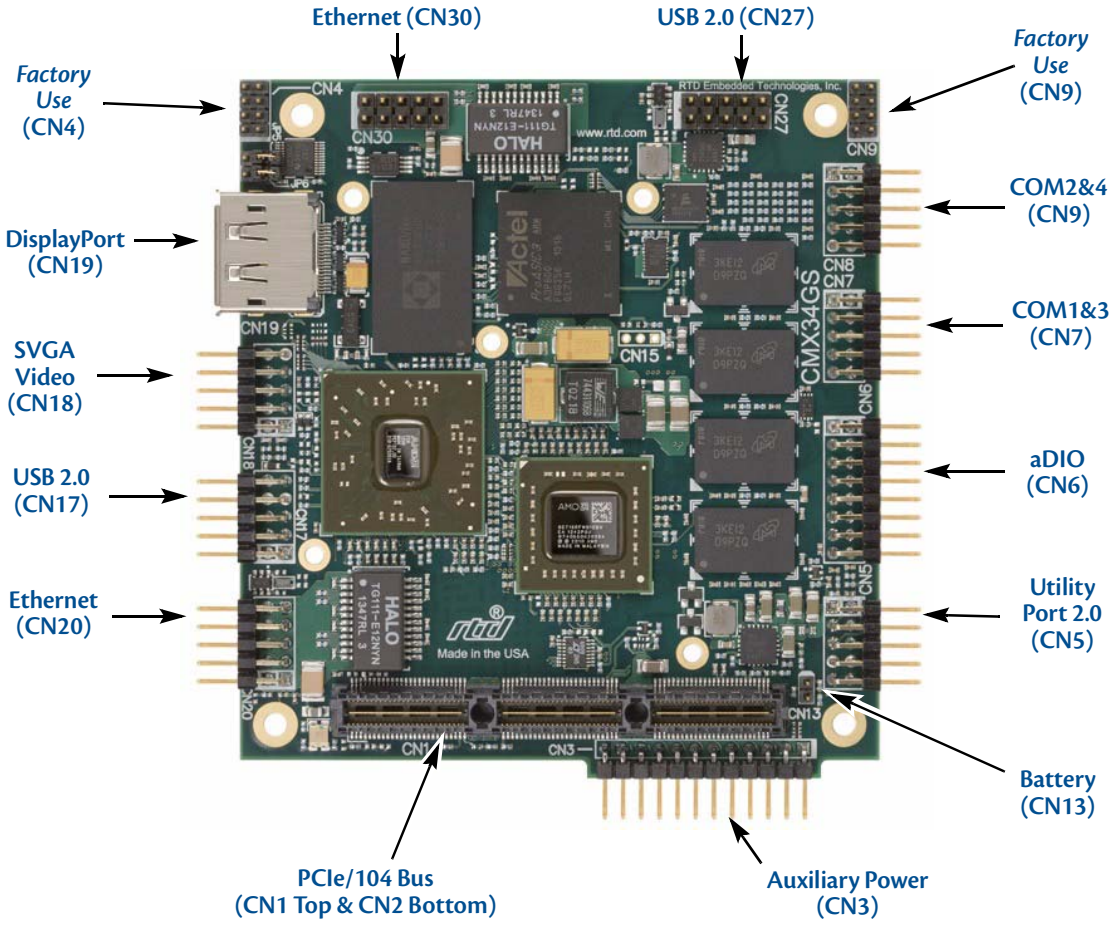


Figure 3 CMX34GS Connector Locations

Note *Pin 1 of each connector is indicated by a white silk-screened square on the top side of the board and a square solder pad on the bottom side of the board.*

Table 7 CMX34GS Basic Connectors

Connector	Function	Size and Pitch	Mating Connector
CN1	PCIe/104 Type 2 Bus (Top)	156-pin, 0.635mm	Samtec ASP-129646-03
CN2	PCIe/104 Type 2 Bus (Bottom)	156-pin, 0.635mm	Samtec ASP-129637-03
CN3	Auxiliary Power	1x12, 0.1"	FCI 65039-025LF
CN5	Utility Port 2.0	2x5, 0.1"	3M 89110-0001
CN6	aDIO	2x8, 0.1"	3M 89116-0001
CN7	Serial Port 1 (COM 1&3)	2x5, 0.1"	3M 89110-0001
CN8	Serial Port 2 (COM 2&4)	2x5, 0.1"	3M 89110-0001
CN13	RTC Battery Input (optional)	1x2, 2mm	FCI 69305-002LF
CN15	Reserved	1x3, 2mm	FCI 69305-003LF
CN17	USB 2.0	2x5, 0.1"	3M 89110-0001
CN18	Video (SVGA)	2x5, 0.1"	3M 89110-0001
CN19	DisplayPort	Molex P/N Series 47272-xxxx	Molex P/N Series 68783-xxxx
CN20	Ethernet	2x5, 0.1"	3M 89110-0001
CN27	USB 2.0	2x5, 0.1"	3M 89110-0001
CN30	Ethernet	2x5, 0.1"	3M 89110-0001

WARNING *If you connect power incorrectly, the module will almost certainly be damaged or destroyed. Such damage is not covered by the RTD warranty! Please verify connections to the module before applying power.*

Power is normally supplied to the cpuModule through the top or bottom PCIe connectors (**CN1** or **CN2**). If you are placing the cpuModule onto a stack that has a PCIe/104 power supply, you do not need to make additional connections to supply power.

Alternatively, if you are using the cpuModule without a PC/104 stack or with a stack that does not include a power supply, refer to *Auxiliary Power (CN3)* on page 28 for an alternative method on how to power the cpuModule.

Selecting the Stack Order for the CMX34GS

There are several things to consider when selecting the order of boards in the stack. Before selecting the order, be sure to determine which bus connector on each board is the "Active" bus. Typically, if a peripheral module has both PCIe and PCI bus connectors, only the PCIe is active and the PCI is pass-through. The following is a list of rules to use to determine the stack order:

1. The PCIe connectors above and below the CPU have completely separate signals. Therefore it is possible to attach boards to the PCIe connector above and below the CPU.
2. Any board that uses a PCIe or SATA link must be within six boards of the CPU.
3. To preserve power integrity, it is recommended that there be no more than six boards between the CPU and the power supply.
4. In order to maintain maximum performance over the full temperature range, it is recommended that a PCIe spacer be used between the CPU and any board immediately above it.
5. A maximum of four PCI boards may be attached to any PCI bus.
6. The PCIe to PCI bridge (if one exists in the stack) must be at one end of the PCI bus segment, and all of the peripheral cards at the other end. There may be up to eight PCI pass-through connectors between the PCIe to PCI bridge and the peripheral cards.
7. There must be no more than two boards between the first PCI peripheral and the last PCI peripheral. If there are four PCI peripheral cards in a PCI bus segment, there may not be any PCI pass-through connections between them.

Stack Example

The figure below shows an example of a complete system stack. Most systems will be a subset of this example. This example stack may be further expanded with PCIe to PCIe bridges, or a PCIe to PCI bridge.

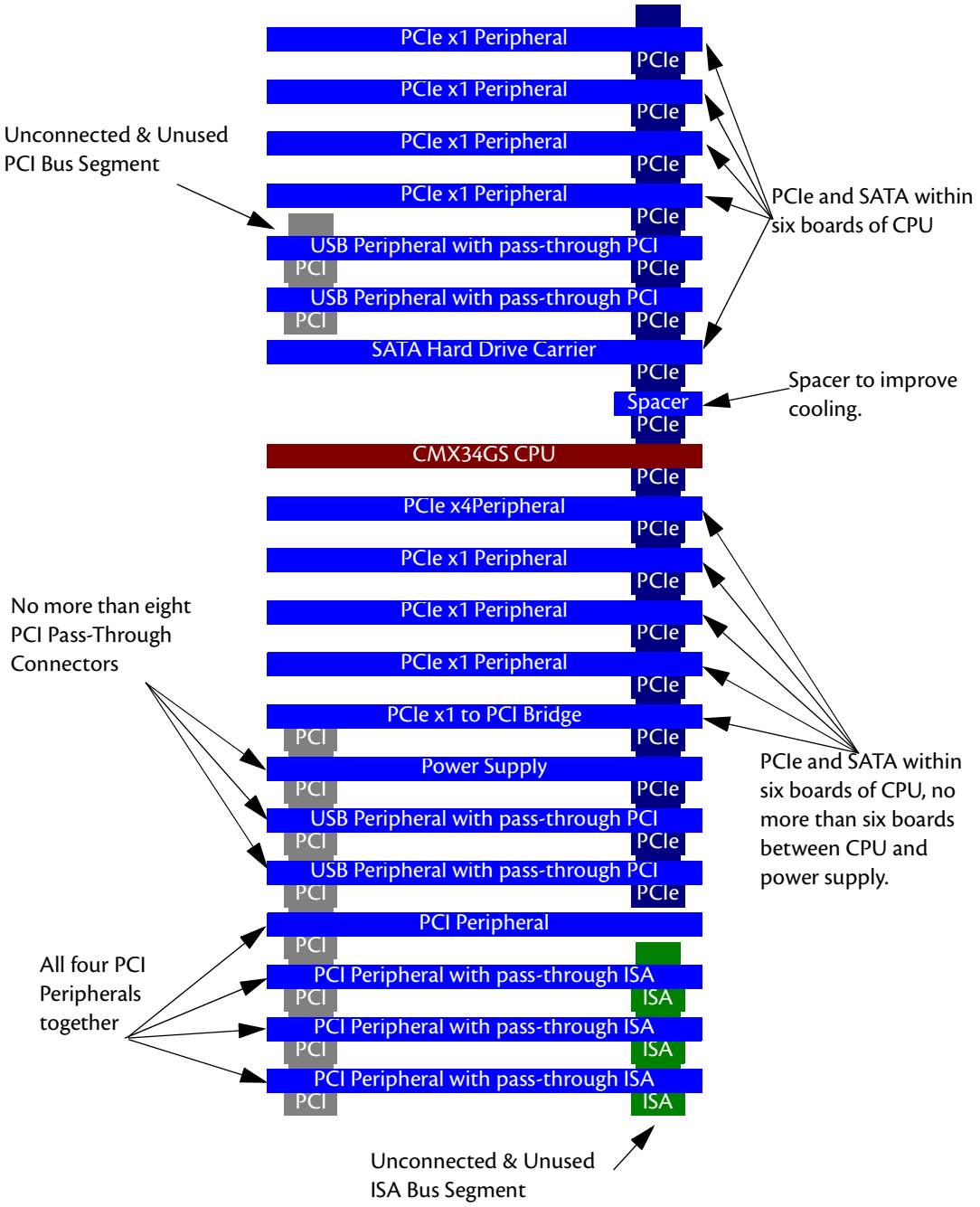


Figure 4 System Stacking Example

Connecting to the Stack

The bus connectors of the cpuModule are simply plugged onto a PC/104 stack to connect to other devices. Follow the procedure below to ensure that stacking of the modules does not damage connectors or electronics.

WARNING *Do not force the module onto the stack! Wiggling the module or applying too much pressure may damage it. If the module does not readily press into place, remove it, check for bent pins or out-of-place keying pins, and try again.*

For mechanical dimensions, including board-to-board spacing, see *Physical Dimensions* on page 78.

1. Turn off power to the PC/104 system or stack.
2. Always work at an ESD protected workstation, and wear a grounded wrist-strap.
3. Select and install stand-offs to properly position the cpuModule on the stack.
4. Remove the cpuModule from its anti-static bag.
5. Check that pins of the bus connector are properly positioned.
6. Check the stacking order; make sure all of the busses used by the peripheral cards are connected to the cpuModule.
7. Hold the cpuModule by its edges and orient it so the bus connector pins line up with the matching connector on the stack.
8. Gently and evenly press the cpuModule onto the PC/104 stack.

Power Input Connections

Power to the board must come from either the top or bottom PCIe/104 Type 2 bus connectors (**CN1** or **CN2**), or the auxiliary power connector (**CN3**). These connectors provide the required +5V and +12V DC voltage rail inputs to the cpuModule.

Connecting to the Utility Port 2.0

The Utility Port 2.0 connector (**CN5**) implements the following interfaces:

- One USB 2.0 (Universal Serial Bus) port
- Speaker port (0.1W output)
- Hardware Reset input
- Battery input for Real Time Clock
- Soft Power Button input

To use these interfaces, you must connect to the Utility Port 2.0 connector (**CN5**). The Utility Port 2.0 cable from the RTD cable kit provides a small speaker, two USB 2.0 ports for a keyboard and mouse, a push-button for resetting the system, a soft-power button, and a lithium battery to provide backup power for the real time clock.

Refer to *Utility Port 2.0 Connector (CN5)* on page 29 to connect devices to the Utility Port 2.0 connector.

Booting the CMX34GS cpuModule for the First Time

You can now apply power to the cpuModule.If you press **Delete** on a keyboard while booting, the cpuModule will enter Setup. Once you have configured the cpuModule using Setup, save your changes and reboot. If you don't press **Delete**, the cpuModule will try to boot from the current settings.

Note *You may miss the initial sign-on messages if your monitor takes a while to power on.*

Note *By default, cpuModules are shipped with a UEFI (Unified Extensible Firmware Interface) shell. When no other bootable device is installed in the system, the system will boot to it exclusively. This internal bootable shell may be disabled in the BIOS screen's boot menu.*

Pressing **F4** on a keyboard while the cpuModule is booting will result in launching a menu display listing the system's bootable devices. This menu permits selecting a different boot device for the power cycle, overriding the boot order settings in the BIOS setup.

Chapter 3 Connecting the cpuModule

This chapter provides information on all CMX34GS cpuModule connectors.

Proper Grounding Techniques — page 26

Connector Locations — page 26

Auxiliary Power (CN3) — page 28

Utility Port 2.0 Connector (CN5) — page 29

SVGA Video Connector (CN18) — page 32

DisplayPort Connector (CN19) — page 33

Serial Port 1 (CN7) and Serial Port 2 (CN8) — page 35

Advanced Digital I/O (aDIO™) Port (CN6) — page 41

USB 2.0 Connectors (CN17 and CN27) — page 42

Ethernet (10/100/1000Base-T and -TX) Connectors (CN20 and CN30) — page 44

PCIe/104 Type 2 Bus (CN1 - Top and CN2 - Bottom) — page 45

Optional RTC Battery Input (CN13) — page 48

Proper Grounding Techniques

Before removing the CMX34GS from its static bag, proper grounding techniques must be used to prevent electrostatic discharge (ESD) damage to the cpuModule. Common grounding procedures include an anti-static mat on a workbench, which may connect to an anti-static wrist strap (also known as an ESD wrist strap) on the wrist of the technician or engineer.

Connector Locations

Figure 5 shows the connectors of the CMX34GS cpuModule.

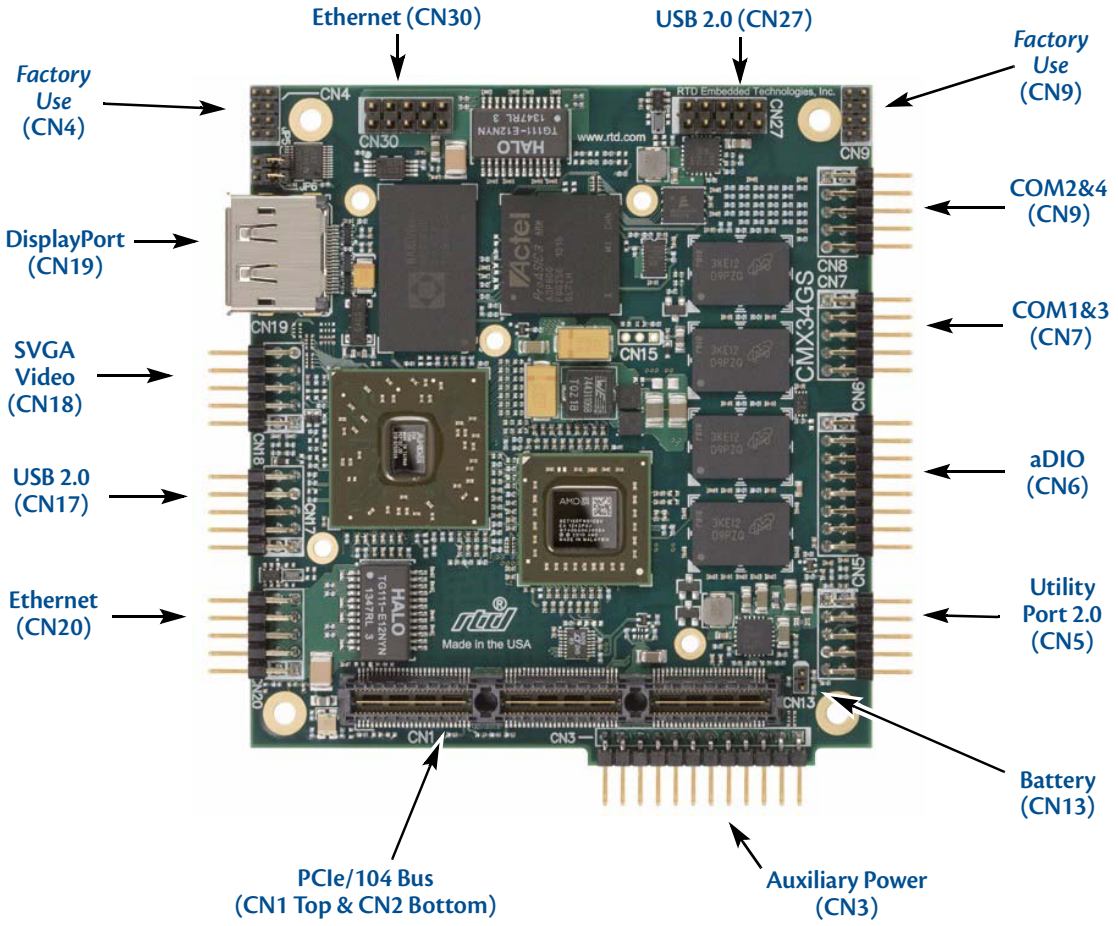


Figure 5 CMX34GS Connector Locations

Note *Pin 1 of each connector is indicated by a white silk-screened square on the top side of the board and a square solder pad on the bottom side of the board. Pin 1 of the bus connectors match when stacking PC/104 modules.*

Table 8 CMX34GS Basic Connectors

Connector	Function	Size and Pitch	Mating Connector
CN1	PCIe/104 Type 2 Bus (Top)	156-pin, 0.635mm	Samtec ASP-129646-03
CN2	PCIe/104 Type 2 Bus (Bottom)	156-pin, 0.635mm	Samtec ASP-129637-03
CN3	Auxiliary Power	1x12, 0.1"	FCI 65039-025LF
CN5	Utility Port 2.0	2x5, 0.1"	3M 89110-0001
CN6	aDIO	2x8, 0.1"	3M 89116-0001
CN7	Serial Port 1 (COM1&3)	2x5, 0.1"	3M 89110-0001
CN8	Serial Port 2 (COM2&4)	2x5, 0.1"	3M 89110-0001
CN13	RTC Battery Input (optional)	1x2, 2mm	FCI 69305-002LF
CN15	Reserved	1x3, 2mm	FCI 69305-003LF
CN17	USB 2.0	2x5, 0.1"	3M 89110-0001
CN18	Video (SVGA)	2x5, 0.1"	3M 89110-0001
CN19	DisplayPort	Molex P/N Series 47272-xxxx	Molex P/N Series 68783-xxxx
CN20	Ethernet	2x5, 0.1"	3M 89110-0001
CN27	USB 2.0	2x5, 0.1"	3M 89110-0001
CN30	Ethernet	2x5, 0.1"	3M 89110-0001

Auxiliary Power (CN3)

The Auxiliary Power connector (**CN3**) can be used to supply power to devices that are attached to the cpuModule. These devices include hard drive, front-end boards for data acquisition systems, and other devices.

Power can also be conveyed to the module through the Auxiliary Power connector (**CN3**). The cpuModule only requires +5 VDC, +12 VDC, and ground for operation.

Note *Although it is possible to power the cpuModule through the Auxiliary Power connector, the preferred method is to power it through the bus connector from a power supply in the stack. The cpuModule can have large current transients during operation, which make powering it through wires difficult. Powering through the bus eliminates such problems as voltage drop and lead inductance.*

If using the Auxiliary Power connector to power the system, care must be taken to ensure good power connections. The power and ground leads must be twisted together, or as close together as possible to reduce lead inductance. A separate lead must be used for each of the power pins. All 5V pins, 12V pins, and all ground pins must be connected. Do not use wire smaller than 20 gauge, and take care to ensure the length of the wire does not exceed 2 ft. The power supply solution must be verified by measuring voltage at the Auxiliary Power Connector and verifying that it meets the input voltage specifications. The voltage at the connector should be checked with an oscilloscope while the system is operational.

WARNING *This 12-pin power connector is **not** compatible with previous generations of RTD cpuModules.*

WARNING *If you connect power incorrectly, the module will almost certainly be destroyed. Please verify power connections to the module before applying power.*

Table 9 Auxiliary Power Connector (CN3)

Pin	Signal	Function
1	GND	Ground
2	+5 V	+5 Volts DC
3	+5 V	+5 Volts DC
4	GND	Ground
5	GND	Ground
6	+12V	+12 Volts DC
7	+12V	+12 Volts DC
8	GND	Ground
9	GND	Ground
10	+5 V	+5 Volts DC
11	+5 V	+5 Volts DC
12	GND	Ground

Utility Port 2.0 Connector (CN5)

The Utility Port 2.0 connector implements the following functions:

- 1x USB 2.0 (Universal Serial Bus) Port
- Speaker port (0.1W output)
- Hardware Reset input
- Soft Power Button input
- Battery input for Real Time Clock

Table 10 provides the pinout of the Utility Por 2.0 connector.

Table 10 Utility Port 2.0 Connector (CN5)

Pin	Signal	Function	In/Out
1	SPKR	Speaker Output (open collector)	out
2	PWR	+5 V	out
3	RESET#	Manual Push-Button Reset	in
4	DATA–	Bidirectional data line for USB1	in/out
5	PWRSW#	Soft Power Button	in
6	DATA+	Bidirectional data line for USB1	in/out
7	GND	Ground	out
8	GND	Ground	out
9	BAT	RTC Battery Input	in
10	GND	Ground	out

WARNING *The pinout of the Utility Port 2.0 connector is* ***not*** *compatible with previous generations of RTD cpuModules. Attaching a legacy Utility Port harness to the Utility Port 2.0 connector may damage or destroy the cpuModule.*

Facing the connector pins, the pinout is:

9	7	5	3	1
BAT	**GND**	**PWRSW#**	**RESET#**	**SPKR**
GND	**GND**	**DATA+**	**DATA-**	**PWR**
10	8	6	4	2

USB 2.0 Connector

One USB 2.0 compliant connector is available on connector **CN5**. Table 10 provides the pinout of the USB connector.

Note *For proper operation at USB 2.0 speeds, be sure to use a cable that is rated for USB 2.0, such as the cable kit supplied by RTD.*

Speaker

A speaker output is available on pins 1 and 2 of the Utility Port 2.0 connector. These outputs are controlled by a transistor to supply 0.1 W of power to an external speaker. The external speaker should have 8 Ohm impedance and be connected between pins 1 and 2.

System Reset

Pin 3 of the Utility Port 2.0 connector allows connection of an external push-button to manually reset the system. The push-button should be normally open, and connect to ground when pushed. The type of reset generated by this button can be set in the BIOS configuration utility.

Soft Power Button

Pin 5 of the Utility Port 2.0 connector allows connection of an external push-button to send a soft power signal to the system. The push-button should be normally open, and connect to ground when pushed. For more information on the modes of the Soft Power Button, refer to the *Power Management* section in Chapter 4, *Using the cpuModule*.

Battery

Pin 9 of the Utility Port 2.0 connector is the connection for an external backup battery. This battery is used by the cpuModule when system power is removed in order to preserve the date and time of the real time clock.

Connecting a battery is only required to maintain time when power is completely removed from the cpuModule. A battery is not required for board operation.

WARNING *The optional RTC battery input connector (**CN13**) should be left unconnected if the multi-function connector (**CN5**) has a battery connected to pin 9.*

SVGA Video Connector (CN18)

Table 11 provides the pinout of the video connector.

Table 11 SVGA Video Connector (CN18)

Pin	Signal	Function	In/Out
1	VSYNC	Vertical Sync	out
2	HSYNC	Horizontal Sync	out
3	DDCSCL	Monitor Communications Clock	out
4	RED	Red Analog Output	out
5	DDCSDA	Monitor Communications Data	bidirectional
6	GREEN	Green Analog Output	out
7	PWR	+5 V	out
8	BLUE	Blue Analog Output	out
9	GND	Ground	out
10	GND	Ground	out

Facing the connector pins of the SVGA Video connector (**CN18**), the pinout is:

9	7	5	3	1
GND	**PWR**	**DDCSDA**	**DDCSCL**	**VSYNC**
GND	**BLUE**	**GREEN**	**RED**	**HSYNC**
10	8	6	4	2

DisplayPort Connector (CN19)

The DisplayPort connector on the CMX34GS cpuModule is a standard PC DisplayPort connector complete with latch holes to provide a rugged connecting solution for latching DisplayPort cables.

The DisplayPort supports all mandatory features of the VESA DisplayPort Standard (Version 1.1a), permits a maximum resolution of 1920x1200, and supports up to 8 channels of audio out the connector. Full bandwidth transmission is supported over a two meter cable, with reduced bandwidth transmission supported up to a length of 15 meters.

The connection supports Dual-Mode DisplayPort (also know as DisplayPort++, sometimes abbreviated as DP++), and can directly output single-link HDMI and DVI signals by using a simple passive adapter. Passive adapters acheive HDMI and DVI signaling by adjusting the lower signal levels output by the connector.

Table 12 provides the pinout of the DisplayPort connector.

Table 12 DisplayPort Connector (CN19)

Pin	Signal	Standard Function	Dual-mode (DP++) Function (DVI / HDMI mode)[1]	In/Out
1	LN0+	Main Link, Lane 0 (positive)	TMDS Channel 2 (positive)	out
2	GND	Ground	Ground	out
3	LN0-	Main Link, Lane 0 (negative)	TMDS Channel 2 (negative)	out
4	LN1+	Main Link, Lane 1 (positive)	TMDS Channel 1 (positive)	out
5	GND	Ground	Ground	out
6	LN1-	Main Link, Lane 1 (negative)	TMDS Channel 1 (negative)	out
7	LN2+	Main Link, Lane 2 (positive)	TMDS Channel 0 (positive)	out
8	GND	Ground	Ground	out
9	LN2-	Main Link, Lane 2 (negative)	TMDS Channel 0 (negative)	out
10	LN3+	Main Link, Lane 3 (positive)	TMDS Clock (positive)	out
11	GND	Ground	Ground	out
12	LN3-	Main Link, Lane 3 (negative)	TMDS Clock (negative)	out
13	CFG1	Configuration Pin 1	Cable Adapter Detect	out
14	CFG2	Configuration Pin 2	Consumer Electronics Control[2]	out
15	AUX+	Auxiliary Channel (positive)	DDC Clock	in/out
16	GND	Ground	Ground	out
17	AUX-	Auxiliary Channel (negative)	DDC Data	in/out
18	HPD	Hot Plug Detect	Hot Plug Detect	in
19	DPG	Return for DPV	Return for DPV	out
20	DPV	+3.3V DC Power	+3.3V DC Power	out

1. Requires special passive adapter
2. HDMI mode only

Facing the connector pins of the DisplayPort connector (**CN19**), the pinout is:

19	17	15	13	11	9	7	5	3	1
DPG	AUX-	AUX+	CFG1	GND	LN2-	LN2+	GND	LN0-	LN0+
DPV	HPD	GND	CFG2	LN3-	LN3+	GND	LN1-	LN1+	GND
20	18	16	14	12	10	8	6	4	2

Serial Port 1 (CN7) and Serial Port 2 (CN8)

Serial Port 1 (COM1) is implemented on connector **CN7**, and Serial Port 2 (COM2) is implemented on connector **CN8**. The serial ports are normally configured as PC compatible full-duplex RS-232 ports, but you may use the BIOS Setup program to reconfigure these ports as half-duplex RS-422 or full-duplex RS-422 or RS-485. If you reconfigure the ports, you must also select the I/O address and corresponding interrupt using Setup. Table 13 provides the standard I/O addresses and corresponding interrupts.

Table 13 Serial Port Settings

I/O Address (hex)	IRQ
03F8	IRQ4
02F8	IRQ3
03E8	IRQ4
02E8	IRQ3

Serial Port UART

The serial ports are implemented with a 16550/16750-compatible UART (Universal Asynchronous Receiver/Transmitter). This UART is capable of baud rates up to 115.2 kbaud, and includes a 64-byte FIFO. Refer to any standard PC-AT hardware reference for the register map of the UART.

RS-232 Serial Port (Default)

The default serial port mode is full-duplex RS-232. With this mode enabled, the serial port connectors must be connected to RS-232 compatible devices. Table 14 provides the serial port connector pinout and shows how to connect to an external DB-25 or DB-9 compatible serial connector.

Table 14 Serial Port in RS-232 Mode

Pin	Signal	Function	In/Out	DB-25	DB-9
1	DCD	Data Carrier Detect	in	8	1
2	DSR	Data Set Ready	in	6	6
3	RXD	Receive Data	in	3	2
4	RTS	Request To Send	out	4	7
5	TXD	Transmit Data	out	2	3
6	CTS	Clear To Send	in	5	8
7	DTR	Data Terminal Ready	out	20	4
8	RI	Ring Indicate	in	22	9
9,10	GND	Signal Ground	—	7	5

Facing the serial port's connector pins, the pinout is:

9	7	5	3	1
GND	**DTR**	**TXD**	**RXD**	**DCD**
GND	**RI**	**CTS**	**RTS**	**DSR**
10	8	6	4	2

RS-422 or RS-485 Serial Port

You may use the BIOS setup utility to configure the serial ports as RS-422 or RS-485. In this case, you must connect the serial port to an RS-422 or RS-485 compatible device.

When using RS-422 mode, you can use the serial ports in either half-duplex (two-wire) or full-duplex (four-wire) configurations.

Note *The cpuModule has a 120 Ohm termination resistor. Termination is usually necessary on all RS-422 receivers and at the ends of the RS-485 bus. Termination resistors can be enabled in the BIOS setup utility.*

When using full-duplex in RS-422 mode, connect the ports as shown in Table 15.

Table 15 Full-Duplex Connections

Port 1	Port 2
RXD+	TXD+
TXD+	RXD+
RXD–	TXD–
TXD–	RXD–

In RS-485 mode, the connection of the ports is always half-duplex, as the transceivers' transmitters are connected to the receivers internally.

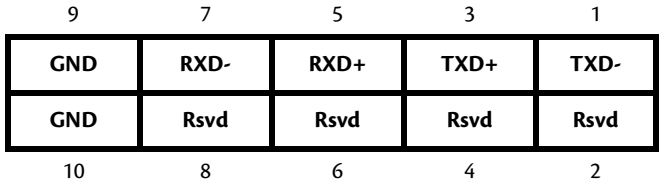
RS-422 Mode Pinout

Table 16 provides the serial port connector pinout when RS-422 mode is enabled.

Table 16 Serial Port in RS-422 Mode

Pin	Signal	Function	In/Out	DB-9
1	TXD–	Transmit Data (–)	out	1
2	—	Reserved	—	6
3	TXD+	Transmit Data (+)	out	2
4	—	Reserved	—	7
5	RXD+	Receive Data (+)	in	3
6	—	Reserved	—	8
7	RXD–	Receive Data (–)	in	4
8	—	Reseved	—	9
9,10	GND	Signal Ground	out	5

Facing the serial port connector, the pinout is:



WARNING *The pinout of the COM ports in RS-422 mode is* ***not*** *compatible with previous generations of RTD cpuModules.*

RS-485 Mode Pinout

Table 17 provides the serial port connector pinout when RS-482 mode is enabled

Table 17 Serial Port in RS-485 Mode

Pin	Signal	Function	In/Out	DB-9
1	D–	Data (–)	in/out	1
2	—	Reserved	—	6
3	D+	Data (+)	in/out	2
4	—	Reserved	—	7
5	—	Reserved	—	3
6	—	Reserved	—	8
7	—	Reserved	—	4
8	—	Reseved	—	9
9,10	GND	Signal Ground	out	5

Facing the serial port connector, the pinout is:

9	7	5	3	1
GND	**Rsvd**	**Rsvd**	**D+**	**D-**
GND	**Rsvd**	**Rsvd**	**Rsvd**	**Rsvd**
10	8	6	4	2

WARNING *The pinout of the COM ports in RS-485 mode is* ***not*** *compatible with previous generations of RTD cpuModules.*

Note *When using the serial port in RS-485 mode, the serial transmitters are enabled and disabled under software control. The transmitters are enabled by manipulating the Request To Send (RTS*) signal of the serial port controller. This signal is controlled by writing bit 1 of the Modem Control Register (MCR) as follows:*

- If MCR bit 1 = 1, then RTS* = 0, and serial transmitters are disabled
- If MCR bit 1 = 0, then RTS* = 1, and serial transmitters are enabled

Note *For more information on the serial port registers, including the MCR, refer to the Serial Port Programming reference in Appendix D.*

Dual Serial Port Modes

The serial port connectors can be configured as dual serial ports in the BIOS. The mapping between the connectors and COM port numbers is shown in Table 18. The supported combinations of serial port modes are listed in Table 19, which also includes a reference to the corresponding connector pinout.

Table 18 Dual Serial Port Connections

Connector	COM A	COM B
CN7	COM 1	COM 3
CN8	COM 2	COM 4

Table 19 Dual Serial Port Modes

COM A	COM B	Pinout Reference	Echo Mode
RS-232	RS-232	Table 20	—
RS-422	RS-422	Table 21	—
RS-485	RS-485	Table 22	echo cancelled
RS-485	RS-485	Table 21	with echo[1]

1. Dual RS-485 mode with echo uses dual RS-422 mode pinout

WARNING *The dual serial port mode pinouts of the COM ports are* ***not*** *compatible with previous generations of RTD cpuModules.*

Note *The cpuModule has 120 Ohm termination resistors. Termination is usually necessary on all RS-422 receivers and at the ends of the RS-485 bus. Termination resistors can be enabled in the BIOS setup utility. When termination is enabled in dual port mode, it is enabled for both ports.*

Table 20 COM A (RS-232) and COM B (RS-232)

Pin	Signal	Function	In/Out	DB-9
1	DCD1	COM A - Data Carrier Detect	in	1
2	DSR1	COM A - Data Set Ready	in	6
3	RXD1	COM A - Receive Data	in	2
4	TXD2	COM B - Transmit Data	out	7
5	TXD1	COM A - Transmit Data	out	3
6	RXD2	COM B - Receive Data	in	8
7	DTR1	COM A - Data Terminal Ready	out	4
8	RI1	COM A - Ring Indicate	in	9
9,10	GND	Signal Ground	—	5

Table 21 COM A (RS-422) and COM B (RS-422)[1]

Pin	Signal	Function	In/Out	DB-9
1	TXD1-	COM A- Transmit Data (–)	out	1
2	TXD2-	COM B - Transmit Data (–)	out	6
3	TXD1+	COM A - Transmit Data (+)	out	2
4	TXD2+	COM B - Transmit Data (+)	out	7
5	RXD1+	COM A - Receive Data (+)	in	3
6	RXD2+	COM B - Receive Data (+)	in	8
7	RXD1-	COM A- Receive Data (–)	in	4
8	RXD2-	COM B - Receive Data (–)	in	9
9,10	GND	Signal Ground	—	5

1. Dual RS-485 mode with echo uses dual RS-422 mode pinout

Table 22 COM A (RS-485) and COM B (RS-485)

Pin	Signal	Function	In/Out	DB-9
1	D1-	COM A- Data (–)	in/out	1
2	D2-	COM B - Data (–)	in/out	6
3	D1+	COM A - Data (+)	in/out	2
4	D2+	COM B - Data (+)	in/out	7
5	—	Reserved	—	3
6	—	Reserved	—	8
7	—	Reserved	—	4
8	—	Reserved	—	9
9,10	GND	Signal Ground	—	5

Advanced Digital I/O (aDIO™) Port (CN6)

Connector **CN6** is configured as an aDIO port. aDIO is 12 digital bits configured as 8-bit programmable and 4-bit port programmable I/O, providing any combination of inputs and outputs. Match, event, and strobe interrupt modes mean no more wasting valuable processor time polling digital inputs. Interrupts are generated when the 8-bit programmable digital inputs match a pattern, or on any value change event. Bit masking allows selecting any subgroup of 8 bits. The strobe input latches data into the bit programmable port and generates an interrupt. Refer to *Advanced Digital I/O Ports (aDIO™)* — page 56 for information on programming the aDIO.

Table 23 aDIO Pinout

CN6 Pin	Function	CN6 Pin	Function
1	P0-0	2	P0-1
3	P0-2	4	P0-3
5	P0-4	6	P0-5
7	P0-6	8	P0-7
9	strobe 0	10	strobe 1
11	P1-0	12	P1-1
13	P1-2	14	P1-3
15	GND	16	+5 V[1]

1. Available during standby.

USB 2.0 Connectors (CN17 and CN27)

Four USB 2.0 compliant connectors are available on connector **CN17** and **CN27**. Table 24 provides the pinout of the USB connectors.

Table 24 USB Connector (CN17)

Pin	Signal	Function	In/Out
1	VCC1	Supply +5 V to USB1	out
2	VCC2	Supply +5 V to USB2	out
3	DATA1–	Bidirectional data line for USB1	in/out
4	DATA2–	Bidirectional data line for USB2	in/out
5	DATA1+	Bidirectional data line for USB1	in/out
6	DATA2+	Bidirectional data line for USB2	in/out
7	GND	Ground	out
8	GND	Ground	out
9	GND	Ground	out
10	GND	Ground	out

Table 25 USB Connector (CN27)

Pin	Signal	Function	In/Out
1	VCC3	Supply +5 V to USB3	out
2	VCC4	Supply +5 V to USB4	out
3	DATA3–	Bidirectional data line for USB3	in/out
4	DATA4–	Bidirectional data line for USB4	in/out
5	DATA3+	Bidirectional data line for USB3	in/out
6	DATA4+	Bidirectional data line for USB4	in/out
7	GND	Ground	out
8	GND	Ground	out
9	GND	Ground	out
10	GND	Ground	out

Note *For proper operation at USB 2.0 speeds, be sure to use a cable that is rated for USB 2.0, such as the cable kit supplied by RTD.*

Facing the connector pins, the pinout of **CN17** is:

9	7	5	3	1
GND	**GND**	**DATA1+**	**DATA1–**	**VCC1**
GND	**GND**	**DATA2+**	**DATA2–**	**VCC2**
10	8	6	4	2

Facing the connector pins, the pinout of **CN27** is:

9	7	5	3	1
GND	**GND**	**DATA3+**	**DATA3–**	**VCC3**
GND	**GND**	**DATA4+**	**DATA4–**	**VCC4**
10	8	6	4	2

Ethernet (10/100/1000Base-T and -TX) Connectors (CN20 and CN30)

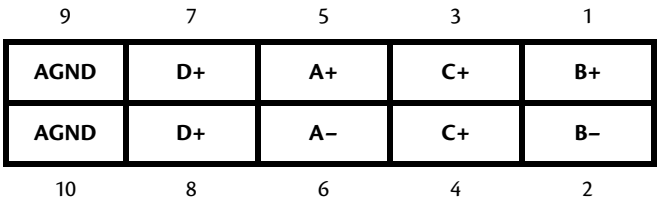
This connector provides a 10/100/1000Base-T Ethernet connection. Table 26 provides the pinout of the Ethernet connector. For 1000Base-T, all four pairs are used for transmit and receive.

To use the onboard 10/100/1000 Ethernet controller, Ethernet must be enabled in the BIOS.

When enabled, the multi-color LED will blink to indicate an Ethernet connection. For more information, refer to the *Multi-Color LED* section on page 69.

Table 26 Ethernet Connector (CN20 and CN30)

RJ-45 Pin	10-Pin DIL Pin	Signal	Function
3	1	B+ (RX+)	Receive+ (10/100)
6	2	B- (RX–)	Receive– (10/100)
4	3	C+	
5	4	C-	
1	5	A+ (TX+)	Transmit+ (10/100)
2	6	A- (TX–)	Transmit– (10/100)
7	7	D+	
8	8	D-	
—	9	AGND	Ethernet Ground
—	10	AGND	Ethernet Ground



PCIe/104 Type 2 Bus (CN1 - Top and CN2 - Bottom)

Connectors **CN1** and **CN2** carry the signals of the PCIe/104 PCIe bus. These signals match definitions found in the **PCI/104-Express & PCIe/104 Specification Version 2.10** from the PC/104 Embedded Consortium. Table 27 lists the pinouts of the PC/104-Express bus connector.

WARNING *Not all PCIe cards are compatible with the PCIe/104 Type 2 connector. Be sure that all of the boards attached to this bus are compatible before powering the system.*

Table 27 PCIe/104 Type 2 Bus Signal Assignments (Top View)[1]

Pin	Signal		Signal	Pin
1	USB_OC#		PE_RST#	2
3	+3.3V		+3.3V	4
5	USB_1p		USB_0p	6
7	USB_1n		USB_0n	8
9	GND		GND	10
11	PEx1_1Tp		PEx1_0Tp	12
13	PEx1_1Tn		PEx1_0Tn	14
15	GND		GND	16
17	PEx1_2Tp		PEx1_3Tp *(CN2 only)*	18
19	PEx1_2Tn		PEx1_3Tn *(CN2 only)*	20
21	GND		GND	22
23	PEx1_1Rp		PEx1_0Rp	24
25	PEx1_1Rn	+5 Volts	PEx1_0Rn	26
27	GND		GND	28
29	PEx1_2Rp		PEx1_3Rp *(CN2 only)*	30
31	PEx1_2Rn		PEx1_3Rn *(CN2 only)*	32
33	GND		GND	34
35	PEx1_1Clkp		PEx1_0Clkp	36
37	PEx1_1Clkn		PEx1_0Clkn	38
39	+5V_STBY		+5V_STBY	40
41	PEx1_2Clkp		PEx1_3Clkp *(CN2 only)*	42
43	PEx1_2Clkn		PEx1_3Clkn *(CN2 only)*	44
45	CPU_DIR		PWRGOOD	46
47	Reserved		Reserved	48
49	Reserved		Reserved	50
51	Reserved		PSON#	52

Table 27 PCIe/104 Type 2 Bus Signal Assignments (Top View)[1]

Pin	Signal		Signal	Pin
53	STK0 / WAKE#		STK1	54
55	GND		GND	56
57	Reserved		Reserved	58
59	Reserved		Reserved	60
61	GND		GND	62
63	Reserved		Reserved	64
65	Reserved		Reserved	66
67	GND		GND	68
69	Reserved		Reserved	70
71	Reserved		Reserved	72
73	GND		GND	74
75	Reserved		Reserved	76
77	Reserved	+5 Volts	Reserved	78
79	GND		GND	80
81	SATA_1Tp		SATA_0Tp	82
83	SATA_1Tn		SATA_0Tn	84
85	GND		GND	86
87	Reserved		Reserved	88
89	Reserved		Reserved	90
91	GND		GND	92
93	Reserved		Reserved	94
95	Reserved		Reserved	96
97	GND		GND	98
99	Reserved		Reserved	100
101	Reserved		Reserved	102
103	GND		GND	104

Table 27 PCIe/104 Type 2 Bus Signal Assignments (Top View)[1]

Pin	Signal		Signal	Pin
105	STK2		Reserved	106
107	GND		GND	108
109	Reserved		Reserved	110
111	Reserved		Reserved	112
113	GND		GND	114
115	Reserved		Reserved	116
117	Reserved		Reserved	118
119	GND		GND	120
121	Reserved		Reserved	122
123	Reserved		Reserved	124
125	GND		GND	126
127	Reserved		Reserved	128
129	Reserved	+12 Volts	Reserved	130
131	GND		GND	132
133	SATA_1Rp		SATA_0Rp	134
135	SATA_1Rn		SATA_0Rn	136
137	GND		GND	138
139	Reserved		Reserved	140
141	Reserved		Reserved	142
143	GND		GND	144
145	Reserved		Reserved	146
147	Reserved		Reserved	148
149	GND		GND	150
151	Reserved		Reserved	152
153	Reserved		Reserved	154
155	GND		GND	156

1. Signals marked with (#) are active low.

PCIe/104 Type 2 Compatibility

The PCIe/104 Type 2 connector is compatible with any PCI/104-Express or PCIe/104 peripheral module that does not use the x16 Link. This includes any card that uses the PCIe x1 links, USB, or a power supply. In addition, this connector can be used to add SATA devices to the system.

If a card is installed that is not compatible with the Type 2 connector, the CPU will keep the system in soft-off, and the LED will be Cyan to indicate that there is a Bus Stacking Error. If this feature is not desired, **JP5** and **JP6** can be installed to disable the Bus Stacking Error feature.

Optional RTC Battery Input (CN13)

The optional RTC battery input is the connection for an external backup battery. This battery is used by the cpuModule when system power is removed in order to preserve the date and time of the real time clock.

Connecting a battery is only required to maintain time when power is completely removed from the cpuModule. A battery is not required for board operation.

Table 28 Optional RTC Battery Input (CN13)

Pin	Signal	Function
1	BAT	RTC Battery Input
2	GND	Ground

WARNING *This optional RTC battery connector (**CN13**) should be left unconnected if the Utility Port 2.0 connector (**CN5**) has a battery connected.*

Chapter 4 Using the cpuModule

This chapter provides information for users who wish to develop their own applications programs for the CMX34GS cpuModule.

This chapter includes information on the following topics:

The RTD Enhanced BIOS — page 50

Operating System Specific Usage — page 52

Memory Map — page 53

I/O Address Map — page 54

Hardware Interrupts — page 55

Advanced Digital I/O Ports (aDIO™) — page 56

SATA Controller Configuration — page 60

Real Time Clock Control — page 62

Watchdog Timer Control — page 65

Thermal Management — page 66

Power Management — page 67

Multi-Color LED — page 69

Reset Status Register — page 70

Features and Settings That Can Affect Boot Time — page 72

System Recovery — page 73

The RTD Enhanced BIOS

The RTD Enhanced BIOS is software that interfaces hardware-specific features of the cpuModule to an operating system (OS). Physically, the BIOS software is stored in a Flash EPROM on the cpuModule. Functions of the BIOS are divided into two parts.

The first part of the BIOS is known as POST (power-on self-test) software, and it is active from the time power is applied until an OS boots (begins execution). POST software performs a series of hardware tests, sets up the machine as defined in Setup, and begins the boot of the OS.

The second part of the BIOS is known as the CORE BIOS. It is the normal interface between cpuModule hardware and the OS which is in control. It is active from the time the OS boots until the cpuModule is turned off. The CORE BIOS provides the system with a series of software interrupts to control various hardware devices.

Configuring the RTD Enhanced BIOS

The cpuModule Setup program allows you to customize the cpuModule's configuration. Selections made in Setup are stored on the board and are read by the BIOS at power-on.

Entering the BIOS Setup

You can run Setup by rebooting the cpuModule and repeatedly pressing the **Delete** key. When you are finished with Setup, save your changes and exit. The system will automatically reboot

Field Selection

To move between fields in Setup, use the keys listed below.

Table 29 Setup Keys

Key	Function
→, ←, ↓, ↑	Move between fields
+, **–**, **PgUp**, **PgDn**	Selects next/previous values in fields
Enter	Go to the submenu for the field
Esc	To previous menu then to exit menu

Main Menu Setup Fields

The following is a list of Main Menu Setup fields.

Table 30 Main Menu Setup Fields

Field	Active Keys	Selections
Main	Press **Enter** to select	Access system information such as the cpuModule's serial number, CPU speed and type, BIOS version, FPGA version, and CMOS time and date settings
Advanced	Press **Enter** to select	Setup advanced RTD cpuModule features, including boot options, aDIO and serial port configuration, and miscellaneous feature control.
AMD	Press **Enter** to select	Setup AMD CPU and chipset features such as power-state control, graphics configurations, and SATA and USB configuration
Security	Press **Enter** to select	Setup the supervisor and user access passwords or enable boot sector virus protection
Boot	Press **Enter** to select	Set the system boot sequence
Exit	Press **Enter** to select	Save or discard changes and exit the BIOS, or load the default BIOS settings

Note *Future BIOS versions may have slightly different setup menus and options.*

Boot Device Selection Menu

Pressing F4 on a keyboard while the cpuModule is booting will result in launching a menu display listing the system's bootable devices. This menu permits selecting a different boot device for the power cycle, overriding the boot order settings in the BIOS setup.

Operating System Specific Usage

Windows®

AMD has identified an issue with Windows 7 where the USB controller can lose synchronization with the main state machine, and may enter a state from which it cannot exit, resulting in a Windows BSOD (Blue Screen of Death). This issue cannot be corrected by installing AMD's drivers, however, it can be resolved with a Windows Registry change. For more information on this workaround, refer to Microsoft® Knowledge Base article ID 982091.

Linux®

The CMX34GS is fully supported with Linux kernel version 3.1 and onward. Using the CMX34GS with previous versions of the kernel will require additional configuration steps to fully utilize video. Specifically, users will need to install the AMD Catalyst™ 13.1 Proprietary Linux® Graphics Driver or later.

Memory Map

Table 31 shows how memory in the first megabyte is allocated in the system.

Table 31 First Megabyte Memory Map

Address (hex)	Description
E0000–FFFFFh	Legacy BIOS image
CF600-DFFFFh	Other ROMs
CE600–CF5FFh	Ethernet Boot PXE ROM
C0000–CE5FFh	Video BIOS
A0000–BFFFFh	Video memory[1]
9D800–9FFFFh	Extended BIOS data area
00500–9D7FFh	DOS reserved memory area
00400–004FFh	BIOS data area
00000–003FFh	Interrupt vector area

1. Depends on video mode

Memory beyond the first megabyte can be accessed in real mode by using EMS or a similar memory manager. See your OS or programming language references for information on memory managers.

I/O Address Map

As with all standard PC/104 boards, the total I/O space is 64k in size. However, because early processors only addressed 10 address lines (SA0–SA9), the first 1k is used for legacy I/O devices. Any ISA add-on modules you install must therefore use I/O addresses in the range of 0–1023 (decimal) or 000–3FF (hex). The upper I/O addresses are used for PCI I/O devices, and are automatically assigned by the BIOS or operating system at boot time.

Note *If you add any peripherals to the system you must ensure they do not use reserved addresses listed below, or malfunctions will occur. The exception to this is if the resource has been released by the user.*

Table 32 lists I/O addresses reserved for the CMX34GS cpuModule.

Table 32 I/O Addresses Reserved for the CMX34GS cpuModule

Address Range (hex)	Bytes	Device
000–00Fh	16	DMA Controller
020–021h	2	Interrupt Controller 1
022–02Fh	13	Reserved
040–043h	4	Timer
060–064h	5	Keyboard Interface
070–071h	2	Real Time Clock Port
080–08Fh	16	DMA Page Register
0A0–0A1h	2	Interrupt Controller 2
0C0–0CFh	16	DMA Controller 2
0F0–0FFh	16	Math Coprocessor
170–17Fh	16	Hard Disk - Secondary Command[1]
1F0–1FFh	16	Hard Disk - Primary Command[1]
200–201h	2	Reserved
2E8–2EFh	8	Serial Port[2]
2F8–2FFh	8	Serial Port[2]
376-377h	2	Hard Disk - Secondary Control[1]
3E8–3EFh	8	Serial Port[2]
3F6-3F7h	2	Hard Disk - Primary Control[1]
3F8–3FFh	8	Serial Port[2]
C00-C6Fh	112	A55E Chipset
CD0-CDFh	16	A55E Chipset
E80-EBFh	64	Reserved
EC0-EC4h	5	aDIO[3]
EC5-EFFh	59	Reserved

1. The I/O addresses listed will only be occupied when the SATA controller is configured for Legacy Mode. When configured for Native Mode (BIOS default), they will be available.
2. The I/O addresses for the serial port are selected in the BIOS Setup utility.
3. If aDIO is disabled, the I/O addresses listed will not be occupied.

Hardware Interrupts

Note *If you add any expansion modules or other peripherals to the system, you must ensure they do not use interrupts needed by the cpuModule, or malfunctions will occur.*

The CMX34GS cpuModule supports the standard PC interrupts listed in Table 33. Interrupts not in use by hardware on the cpuModule itself are listed as available. Similarly, if the operating system is using APIC, more IRQs will be available.

Table 33 Hardware Interrupts Used on the CMX34GS cpuModule

Interrupt	Normal Use
0	Timer 0
1	Keyboard
2	Cascade of IRQ 8–15
3	COM2
4	COM1
5	Available
6	Available
7	Available
8	Real Time Clock
9	Available, routed to IRQ 2
10	Available
11	Available
12	Available
14[1]	Available[1]
15[1]	Available[1]

1. IRQs 14 and 15 are available when the SATA controller is configured in Native Mode (BIOS default), but will be utilized the SATA controller is configured for Legacy Mode.

Note *The cpuModule has onboard PCI devices that will claim IRQ lines. In some instances, a PCI device will claim an IRQ line that is required by a legacy device.*

Note *A device's hardware interrupt will be available for use if the given device is not present in the system and the device is disabled in the BIOS setup utility.*

Advanced Digital I/O Ports (aDIO™)

This board supports 12 bits of TTL/CMOS compatible digital I/O (TTL signaling). These I/O lines are grouped into two ports, Port 0 and Port 1. Port 0 is bit programmable; Port 1 is byte programmable. Port 0 supports RTD's Advanced Digital Interrupt modes. The three modes are strobe, match and event. Strobe mode generates an interrupt and latches Port 0 when the strobe input transitions from low to high. Match mode generates an interrupt when an 8-bit pattern is received in parallel that matches the match mask register. Event mode generates an interrupt when a change occurs on any bit. In any mode, masking can be used to monitor selected lines.

When the CPU boots, all digital I/O lines are programmed as inputs, meaning that the digital I/O line's initial state is undetermined. If the digital I/O lines must power up to a known state, an external 10 k-Ohm resistor must be added to pull the line high or low.

The 8-bit control read/write registers for the digital I/O lines are located from I/O address EC0h to EC3h. These registers are written to zero upon power up. From EC0h to EC3h, the name of these registers are **Port 0 data**, **Port 1 data**, **Multi-Function**, and **DIO-Control** register.

Note *While the 16-pin aDIO connector is pin-for-pin compatible with previous generations of RTD cpuModules (such as the Montevina series), the hardware is slightly different, and requires that writes ands reads to/from the aDIO ports happen no more than once per millisecond. Migrating legacy software to the G-Series that utilizes RTD's Advanced Digital I/O may require that you add this delay prior to all reads and writes.*

Note *RTD provides drivers that support the aDIO interface on popular operating systems. RTD recommends using these drivers instead of accessing the registers directly.*

Digital I/O Register Set

Table 34 Port 0 Data I/O Address EC0h

D7	D6	D5	D4	D3	D2	D1	D0
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Port 0 Data register is a read/write bit direction programmable register. A particular bit can be set to input or output. A read of an input bit returns the value of port 0. A read of an output bit returns the last value written to Port 0. A write to an output bit sends that value to port 0.

Table 35 Port 1 Data I/O Address EC1h

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	P1.3	P1.2	P1.1	P1.0

Port 1 Data register is a read/write byte direction programmable register. A read on this register when it is programmed to input will read the value at the aDIO connector. A write on this register when it is programmed as output will write the value to the aDIO connector. A read on this register when it is set to output will read the last value sent to the aDIO connector.

Table 36 Multi-Function I/O Address EC2h

D7	D6	D5	D4	D3	D2	D1	D0

The multi-function register is a read/write register whose contents are set by the DIO-Control register. See the DIO-Control register description for a description of this register.

Table 37 DIO-Control I/O Address EC3h—Read Access

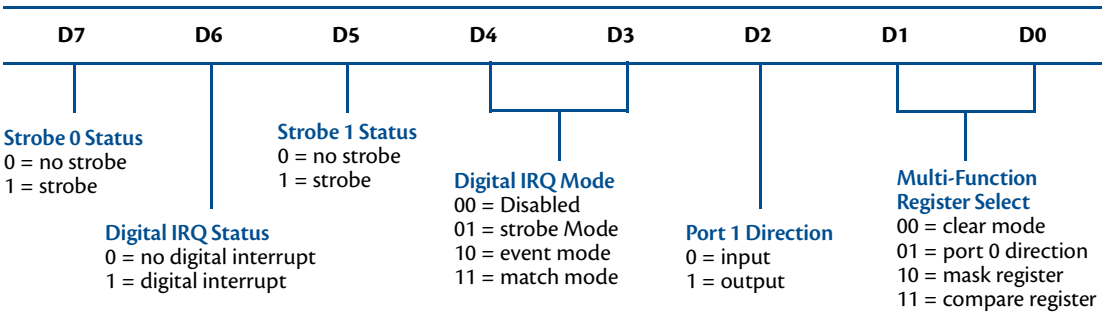


Table 38 DIO-Control I/O Address EC3h—Write Access

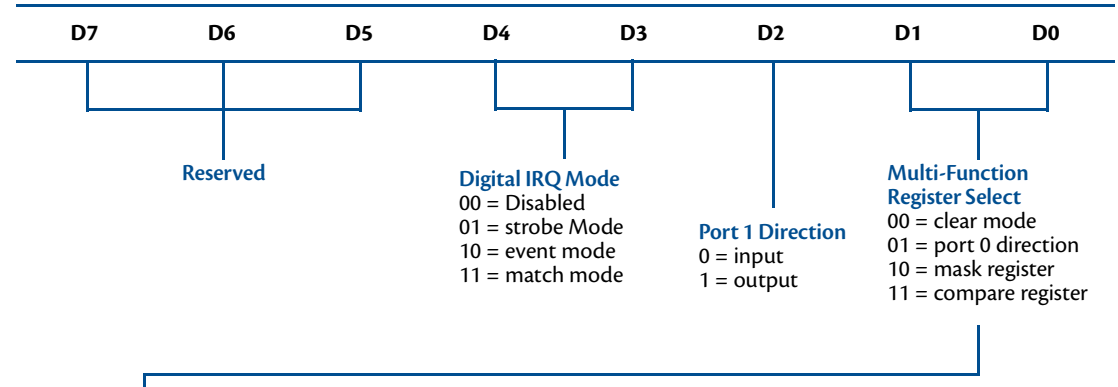


Table 39 Multi-Function at Address EC2h[1]

read/write	00 clear	X	X	X	X	X	X	X	X
0 in, 1 out	01 Port 0 direction	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
0 no mask, 1 mask	10 DIO mask	M7	M6	M5	M4	M3	M2	M1	M0
read/write	11 compare	C7	C6	C5	C4	C3	C2	C1	C0

1. Contents based on bits D0 and D1 of DIO-Control.

Clear Register:

A read to this register Clears the IRQs and a write to this register sets the DIO-Compare, DIO- Mask, DIO-Control, Port 1, and Port 0 to zeros. A write to this register is used to clear the board.

Port 0 Direction Register:

Writing a zero to a bit in this register makes the corresponding pin of the aDIO connector an input. Writing a one to a bit in this register makes the corresponding pin of the aDIO connector an output.

Mask Register:

Writing a zero to a bit in this register will not mask off the corresponding bit in the DIO-Compare register. Writing a one to a bit in this register masks off the corresponding bit in the DIO-Compare register. When all bits are masked off the aDIOs comparator is disabled. This condition means Event and Match mode will not generate an interrupt. This register is used by Event and Match modes.

Compare Register:

A Read/Write register used for Match Mode. Bit values in this register that are not masked off are compared against the value on Port 0. A Match or Event causes bit 6 of DIO-Control to be set and if the aDIO is in Advanced interrupt mode, the Match or Event causes an interrupt.

Port 1 Data register is a read/write byte direction

Interrupts

In order to use an interrupt with aDIO, the interrupt must first be selected in the BIOS setup utility under **Advanced, I/O Devices, aDIO Configuration, aDIO Interrupt**. The Digital I/O can use interrupts 3, 5, 6, 10, and 11. To configure the aDIO interrupt, navigage to the BIOS Setup option, the "Advanced", "RTD aDIO", and "aDIO Interrupt" menu options. The BIOS will automatically reserve the selected interrupt so that is it not assigned to PCI devices. Then, select the appropriate interrupt mode in the DIO Control register.

Advanced Digital Interrupts

There are three Advanced Digital Interrupt modes available. These three modes are Event, Match, and Strobe. The use of these three modes is to monitor state changes at the aDIO connector. Interrupts are enabled by writing to the **Digital IRQ Mode** field in the **DIO-Control** register.

Event Mode

When this mode is enabled, Port 0 is latched into the DIO-Compare register at 8.33 MHz. The aDIO circuitry includes deglitching logic. The deglitching requires pulses on Port 0 to be at least 120 ns in width. As long as changes are present longer than that, the event is guaranteed to register. Pulses as small as 60 ns can register as an event, but they must occur between the rising and falling edge of the 8.33 MHz clock. To enter Event mode, set bits [4:3] of the DIO-Control register to "10".

Match Mode

When this mode is enabled, Port 0 is latched into the DIO-Compare register at 8.33 MHz. The aDIO circuitry includes deglitching logic. The deglitching requires pulses on Port 0 to be at least 120 ns in width. As long as changes are present longer than that, the match is guaranteed to register. Pulses as small as 60 ns can register as a match, but they must occur between the rising and falling edge of the 8.33 MHz clock. To enter Match mode, set bits [4:3] of the DIO-Control register to "11".

Note *Make sure bits [4:3] are set BEFORE writing the DIO-Compare register. If you do not set them first, the contents of the DIO-Compare register could be lost because the Event mode latches in Port 0 into the DIO-Compare register.*

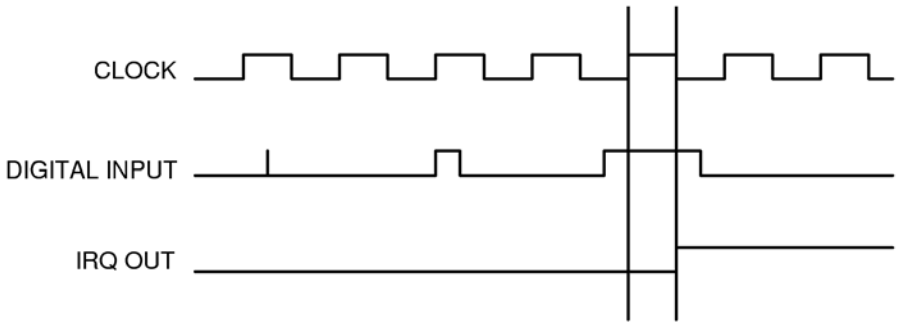


Figure 6 aDIO Match Mode

Strobe Mode

Another interrupt mode supported by aDIO is Strobe mode. This allows the strobe pin of the DIO connector to trigger an interrupt. A low to high transition on the strobe pin will cause an interrupt request. The request will remain high until the Clear Register is read from. Additionally, the Compare Register latched in the value at Port 0 when the Strobe pin made a low to high transition. No further strobes will be available until a read of the Compare Register is made. You must read the Compare Register, and then clear interrupts so that the latched value in the compare register is not lost. To enter Strobe mode, set bits [4:3] of the DIO-Control register to “01”.

SATA Controller Configuration

The CMX34GS has a combined total of five IDE-mode SATA links, each permitting SATA revision 2.0 transfer rates up to 3.0 Gbit/sec. Because IDE-mode controllers allow a maximum of four devices (primary and secondary channels, each supporting a master and slave), the five links are distributed across two controllers.

Four SATA links reside on the top and bottom PCIe/104 Type 2 connectors (**CN1** and **CN2**), and can be enabled/disabled as a group via the BIOS setup. These four links reside behind the same SATA controller on the chipset.

The fifth SATA link connects to the onboard SATA storage, and resides on a dedicated PATA controller, independent from the SATA links on the top and bottom-side PCIe/104 Type 2 connectors. This permits it to be indepently enabled/disabled through the BIOS setup.

SATA Port Mappings, by Connector

Table 40 shows the SATA port configuration of the CMX34GS cpuModule:

Table 40 SATA Port Layout

Controller	Designator	Physical Position, Index	A55E Port Index	Channel Assignment (Legacy Mode)
SATA	**CN1**	PCIe/104 Top, SATA Link 0	3	Secondary Slave
	CN1	PCIe/104 Top, SATA Link 1	2	Primary Slave
	CN2	PCIe/104 Bottom, SATA Link 0	0	Primary Master
	CN2	PCIe/104 Bottom, SATA Link 1	1	Secondary Master
PATA	**n/a**	Onboard SATA storage	4	Primary Master

Onboard SATA Storage

The cpuModule was designed to be used in embedded computing applications. In such environments, rotating media like hard disks and floppy disks are not very desirable. It is possible to eliminate rotating storage devices by placing your operating system and application software into the cpuModule's onboard SATA storage.

The onboard SATA storage will always be connected through the PATA controller, meaning it it will always be shown as a PATA IDE device, and will always be configured for Legacy Mode.

SATA Links on the PCIe/104 Type Connectors

The SATA links on the top and bottom-side PCIe/104 Type connectors (**CN1** & **CN2**) are connected to a SATA controller which can be configured for either Native Mode or Legacy Mode in the BIOS Setup. However, the operating system must support the selected mode for the device to operate correctly. The default configuration for the controller is Native Mode.

Native Mode

Native mode is the default configuration of the onboard SATA controller. Native Mode allows more flexibility than Legacy Mode, as it permits the system to modify the resources used by the SATA controller. When in Native Mode, the SATA controller only requires a single IRQ. Unlike Legacy Mode, this IRQ may be changed by the user or the operating system for better distribution of the system IRQs. When IRQs in the system are more evenly distributed, interrupt latency is minimized. The base address of the controller may also be modified.

Legacy Mode

When in this mode, the controller will be fixed to use two interrupts: IRQs 14 and 15. Similarly, the I/O address of the controller will be fixed in the system. When in Legacy Mode, only a primary and secondary channel may be used in the system.

Note *Because Legacy Mode permits only a primary and secondary channel in the system, configuring the PCIe/104 connector's SATA links for Legacy Mode will disable the onboard SATA storage.*

Real Time Clock Control

Overview

The cpuModule is equipped with a Real Time Clock (RTC) which provides system date and time functions. When the cpuModule is turned off, a battery must be attached to the Utility Port 2.0 connector (**CN5**) to provide power to the RTC. Without power, the RTC will lose the date/time information when the system is turned off.

The RTC also provides an "alarm" function. This may be used to generate an interrupt at a particular time and day. This feature is commonly used to wake up the system from Sleep/Standby to run a scheduled task (defragment the hard drive, back up files, etc.).

In addition to the date/time/alarm functions, the RTC contains several bytes of battery-backed RAM, commonly called CMOS memory. In a typical desktop PC, the CMOS memory is used by the BIOS to store user settings. This RTD cpuModule uses onboard flash to store user BIOS settings. Except for a few well-known CMOS locations which are automatically populated for legacy compatibility, the CMOS memory is largely unused and should be considered "Reserved".

Note *Alternative battery inputs reside on the Optional RTC Battery Input (**CN13**) as well as the PCIe/104 Type 2 Bus connectors (**CN1** & **CN2**).*

WARNING *Only one RTC battery input connection should be used at a time. The other should remain unconnected.*

Accessing the RTC Registers

You may access the RTC date/time and CMOS memory using the Index and Data Registers located at I/O addresses 70h and 71h.

- Address 70h is the Index register. It must be written with the number of the register to read or write. Valid values are 00h to 7Fh.
- Address 71h is the Data register. It contains the contents of the register pointed to by the Index.

To read/write an RTC register, you must first set the Index register with the register number, and then read/write the Data register.

A list of key RTC registers is shown in Table 41 below. This is not an exhaustive list. Refer to the AMD A55E datasheet for more detail.

Table 41 Real Time Clock Registers

Registers (hex)	Registers (decimal)	Function
00h	0	RTC Seconds (BCD format)
02h	2	RTC Minutes (BCD format)
04h	4	RTC Hours (BCD format)
06h	6	RTC Day of Week (BCD format)
07h	7	RTC Day of Month (BCD format)
08h	8	RTC Month (BCD format)
09h	9	RTC Year (BCD format)

Table 41 Real Time Clock Registers

Registers (hex)	Registers (decimal)	Function
0Ah	10	RTC Status Register A • **Bit 7:** RTC Update In Progress (Read Only) - RTC registers should not be accessed when this bit is high. If this bit is low, you have at least 244usec to access the RTD registers. • **Bits 6-5:** Reserved • **Bit 4:** CMOS Bank Selection (0 = Bank 0, 1 = Bank 1) • **Bits 3-0:** Rate select for periodic interrupt.
0Bh	11	RTC Status Register B • **Bit 7:** Set New Time - When high, the RTC is prevented from updating. Set this bit before adjusting system time. • **Bit 6:** Periodic Interrupt Enable - When high, the RTC IRQ will be asserted by the periodic interrupt. • **Bit 5:** Alarm Interrupt Enable - When high, the RTC IRQ will be asserted when the current time matches the alarm time. • **Bit 4:** Update Ended Interrupt Enable - When high, the RTC IRQ will be asserted every time the RTC updates (once per second). • **Bits 2-3:** Reserved • **Bit 1:** Hours Byte Format - Sets the hour byte to 12 or 24 hour time (0=12 hour, 1=24 hour). This is typically set to 24 hour mode. • **Bit 0:** Daylight Savings Enable - When high, the RTC will automatically update itself for Daylight Savings Time. It is recommended to leave this bit low and let the operating system manage time zones and DST.
0Ch	12	RTC Status Register C (Read Only) • **Bit 7:** IRQ Flag - Indicates that the Real Time Clock IRQ is asserted. Goes high whenever one of the enabled interrupt conditions in Register B occurs. • **Bit 6:** Periodic Flag • **Bit 5:** Alarm Flag • **Bit 4:** Update Ended Flag • **Bit 3-0:** Reserved Reading this register will also clear any of set flag (IRQ, Periodic, Alarm, Update Ended). Note that even if the interrupt source is not enabled in Register B, the flags in Register C bits 4, 5, and 6 may still be set.
0Dh	13	RTC Status Register D • **Bit 7:** Valid Time/Date • **Bit 6:** Reserved • **Bits 5-0:** RTC Alarm Day of the Month
32h	50	RTC Century (BDC format); if RTC Status Register A, Bit 4 = 0
48h	72	RTC Century (BDC format); if RTC Status Register A, Bit 4 = 1

Note *RTC registers that are not listed above are used by the BIOS and should be considered "Reserved". Altering the contents of any unlisted RTC register may interfere with the operation of your cpuModule. The specific uses of the unlisted RTC registers will depend on the BIOS version loaded on the cpuModule. Contact RTD's technical support for more information.*

Watchdog Timer Control

The cpuModule includes a Watchdog Timer, which provides protection against programs "hanging", or getting stuck in an execution loop where they cannot respond correctly. The watchdog timer consists of a counter, a reset generator, and an interrupt generator. When the counter reaches the interrupt time-out, it can generate an interrupt. When the counter reaches the reset time-out, the system is reset. The counter is "refreshed," or set back to zero by reading from a specific register. The watchdog can also be put into an "inactive" state, in which no resets or interrupts are generated.

The ability to generate an interrupt allows the application to gracefully recover from a bad state. For example, consider a system that has a reset time-out of 2 seconds, interrupt time-out of 1 second, and the watchdog timer is refreshed every 0.5 seconds. If something goes wrong, an interrupt is generated. The Interrupt service routine then attempts to restart the application software. If it is successful, the application is restarted in much less time than a full reboot would require. If it is not successful, the system is rebooted.

Due to system latency, it is recommended that the Watchdog be refreshed at about half of the reset time-out period, or half of the interrupt time-out period, whichever is applicable.

Register Description

The Advanced Watchdog Timer has a Setup Register and a Runtime Register. The Setup Register is set by the BIOS, and can be adjusted by entering the BIOS Setup Utility, and going to "Advanced", "RTD Advanced Options", "RTD Miscellaneous Feature Control". The Setup Register may also be read by the driver to determine if the Watchdog is enabled, and the interrupt and base address that it is using.

Note *Enabling the watchdog timer in the BIOS does not actually arm it. The watchdog timer can be armed by accessing I/O address E85h, as explained below.*

Table 42 Advanced Watchdog Setup Register E8Bh

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				WDT_IRQ Select Interrupt for WDT 000 = Disabled 001 = IRQ5 010 = Reserved 011 = IRQ10 100 = IRQ11 101 = Reserved 110 = IRQ3 111 = IRQ6			Reg_Enable 0 = Watchdog timer is disabled and Runtime Register will not appear in I/O map 1 = Watchdog Timer is enabled. Runtime Register will appear in I/O map

Table 43 Advanced Watchdog Runtime Register E85h

D7	D6	D5	D4	D3	D2	D1	D0
WDT_Active 0 = Watchdog timer is disabled. 1 = Watchdog is armed and can generate resets and interrupts.	WDT_IRQ_Ena 0 = Watchdog interrupt is disabled. 1 = Watchdog interrupt is enabled.	Reserved		WDT_IRQ_Time Select Interrupt time for WDT 00 = 0.25s 01 = 0.50s 10 = 0.75s 11 = 1.00s		WDT_RST_Time Select Reset time for WDT 00 = 2.00s 01 = 0.50s 10 = 0.75s 11 = 1.00s	

Reading the Runtime Register also refreshes the watchdog timer.

Thermal Management

The cpuModule has several thermal features which can be used to monitor and control the board's temperature when extreme operating conditions are prevalent.

Thermal Monitor

The Thermal Monitor is a feature on the CMX34GS that automatically throttles the CPU when the CPU exceeds its thermal limit. The maximum temperature of the processor is defined as the temperature that the Thermal Monitor is activated. The thermal limit and duty cycle of the Thermal Monitor cannot be modified.

Note *The CPU and PCB temperatures displayed in the BIOS are approximate and should not be used to validate a cooling solution.*

Hardware-Enforced Thermal Protection

The processor includes a hardware-enforced thermal protection mechanism which will cause the processor to enter a Thermal Trip state when the processor's temperature has approached the point at which may be damaged.

Upon entering the Thermal Trip state, the CMX34GS will immediately transition to the **S5** (Soft-Off) ACPI power state. To exit theThermal Trip state (and S5), a power cycle or RSM reset (deepest reset) is required. The reset may be configured as an RSM reset (default BIOS setting) in the BIOS setup utility. For more information on the S5 power state, refer to *Advanced Configuration and Power Interface (ACPI)* — page 67.

The reset status register contains a bit which indicates if the cpuModule has entered S5 as a result of the processor entering the Thermal Trip state. For more information on the reset status register, refer to *Reset Status Register* — page 70.

Further Temperature Reduction

The cpuModule's temperature is directly related to power consumption. Reducing the power consumption of the cpuModule will have an effect on the cpuModule's temperature. Suggested methods for reducing the cpuModule's power consumption can be found in the *Power Management* section on page 67.

Power Management

The CMX34GS cpuModule supports various powering mechanisms which allow the cpuModule to monitor power consumption and temperature, and achieve minimal power consumption states. These unique features include thermal monitoring and thermal throttling, as well as low power modes including ACPI configurations. Various wake options are also available to resume normal system power.

Advanced Configuration and Power Interface (ACPI)

The cpuModule supports several different ACPI low power modes, including the S3, S4, and S5 sleeping states. These suspend modes are described below:

- **S3 (Suspend to RAM):** Everything in the system is powered off except for the system memory. When the system wakes from this mode, operating systems allow applications to resume where they left off, as the state of the application is preserved in memory.
- **S4 (Hibernate):** When the system enters this state, the operating system will save the current state of applications and relevant data to disk, thus allowing the system RAM to be powered down.
- **S5 (Soft-Off):** The system is in a soft off state, and must be rebooted when it wakes.

Power Button Modes

The soft power button input of the Utility Port 2.0 connector (**CN5**) can be configured by the operating system as a suspend button (transition to S3) or as soft power button (transition to S5). Consult your operating system documentation for information on how to configure it. The power button will always cause a transition to S5 if pressed for 4 seconds or longer, without interaction from the operating system.

The soft power button of the Utility Port 2.0 connector (**CN5**) is the only mechanism to wake the system from S4 and S5.

Note *When the reset button of the Utility Port 2.0 connector is configured as a power button (via the BIOS setup utility), it inherits the ACPI suspend and resume features of the power button.*

Low-Power Wake Options

The cpuModule supports several methods of waking from a low power state.

- **Resume from USB:** Operating systems that support S3 permit waking the system from the USB interfaces. Common USB wake methods include insertion of a USB device, a USB keyboard stroke, or movement from another USB device, such as mouse.
- **Resume on RTC Alarm / Timeout:** The RTC Alarm allows the system to turn on at a certain time every day.
- **Resume on WAKE#:** The system can wake when a signal is applied to the WAKE# signal on the PCIe/104 Type 2 connectors (**CN1** & **CN2**).

Table 44 Supported ACPI Resume/Wake Mechanisms

Resume/Wake Mechanism	S3	S4	S5
Wake from USB	Y	—	—
Wake from RTC Alarm / Timeout	Y	—	—
Wake from WAKE# (**CN1** & **CN2**)	Y	—	—
Power Button Input (**CN5**)	Y	Y	Y

Performance States (P-states)

The AMD G-Series processor on the CMX34GS supports various operational performance states (P-states) that are characterized by a combination of the processor's core frequency and voltage. For each processor type, **P0** is the highest-power and highest-performance P-state of the processor. Each ascending P-state number represents a lower-power, lower-performance P-state.

The BIOS setup includes options to set whether the processor operates using higher or lower performance P-States. The default setting is an automatic mode where P-states are entered and exited dynamically based on internal processor core thermal limits and power-monitoring approximations.

The number of P-states varies based on the cpuModule's processor. Each processor's P-states and their corresponding frequencies are shown in the table below:

Table 45 CPU Core Frequencies per P-state

Part Number	Cores	Core Frequency	P0	P1	P2	P3
CMX34GSD1000	Two	1000 MHz	1333 MHz[1]	1000 MHz	800 MHz	615 MHz
CMX34GSS615	One	615 MHz	615 MHz	—	—	—

1. In the P0 P-State, only one core of the dual core processor will see the CPU's boost frequency of 1333 MHz. The other will see 1 GHz.

AT vs. ATX Power Supplies

Both AT and ATX power supplies may be used with the CMX34GS cpuModule, however AT power supplies do not provide any standby power to the cpuModule. When an AT power supply is used to power the system, low power modes that require a standby power to wake the system will not be fully supported.

ATX power supplies do provide a standby power, thus allowing the system to utilize all low power modes supported by the hardware. When an ATX supply is used to power the cpuModule, lower power modes can be achieved. During these low power modes, the standby power from the ATX power supply provides power to a small circuit on the CPU, which is used to watch for a system wake event.

ATX Power Supply Signals

The PCIe/104 Type 2 Bus connectors (**CN1** & **CN2**) provide two ATX style signals., +5V Standby and PSON#. The +5V Standby rail is used to power certain parts of the cpuModule when the main power supply is turned off, i.e. during Suspend-to-RAM (S3), Hibernate (S4), or Soft-Off (S5) power modes. The PSON# signal is an active low open-drain output that signals the power supply to turn on. Use of these signals allows the power consumption to drop to below 1W during standby modes, and still enable any of the wake events.

Reducing Power Consumption

In addition to the CPU's low power modes, power consumption can further be reduced by making some modifications to the BIOS setup. When the following features are disabled in the BIOS, the CPU's power consumption will decrease:

- **Ethernet**
- **USB Ports**
- **SATA Controller**
- **Serial Ports**
- **Multi-Color LED**

Multi-Color LED

The CMX34GS has a Multi-Color LED which can be enabled or disabled in the BIOS setup screen. The color of the LED indicates the status of the board, as shown in Table 46.

Table 46 LED Colors

Color	Description
Green	Normal Operation
Blue	SATA Activity
Red[1]	cpuModule is in reset[2]
Yellow (Red + Green)	cpuModule is in Standby
White (R+G+B)	cpuModule is approaching thermal limit[3]
Cyan (Blue + Green)	Ethernet Link at 100 Mbps or Bus Stacking Error
Magenta (Blue + Red)	Ethernet Link at 1000 Mbps
Blink	Ethernet Activity

1. If power is applied to the cpuModule while jumper **JP5** is installed, the LED will be red. This does not indicate that the board is in reset
2. Unlike previous generations of RTD cpuModules, the CMX34GS requires both +5V and +12V to be present to come out of reset. For more information, refer to: *Auxiliary Power (CN3)* — page 28
3. The LED will remain White until the system is shut down.

The LED can also be controlled manually by writing to I/O Port EA5h, as shown in Table 47 and Table 48.

Table 47 Multi-Color LED I/O Address EA5h

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Multi-Color LED**		

The following table lists the color displayed and the value written.

Table 48 Manual LED Colors

I/O Port 984h Value	Color
0x00	Automatic (see Table 46)
0x08	Off (will reduce system power consumption)
0x09	Blue
0x0A	Green
0x0B	Cyan (Green + Blue)
0x0C	Red
0x0D	Magenta (Red + Blue)
0x0E	Yellow (Red + Green)
0x0F	White (Red + Green + Blue)

Reset Status Register

The cpuModule has several different signals on board which can cause a system reset. If a reset occurs, the reset status register can be used to see which reset or resets have been asserted on the cpuModule.

The user has the ability to see which resets have been asserted. Resets can also be cleared.

- **Examine Resets**: Reading from I/O port 0xEA8 will indicate if a reset has been asserted. If a 1 is read, the corresponding reset has been asserted. If a 0 is read from the bit, the reset has not been asserted
- **Clear Reset**: Each reset can be cleared by writing a 1 to the selected bit of I/O port 0xEA8.

Table 49 Reset Status I/O Address EA8h - Read Access

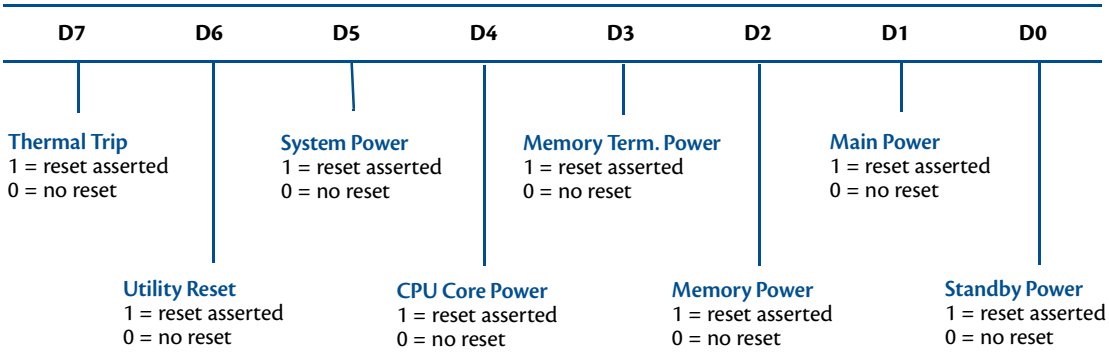


Table 50 Reset Status I/O Address EA8h - Write Access

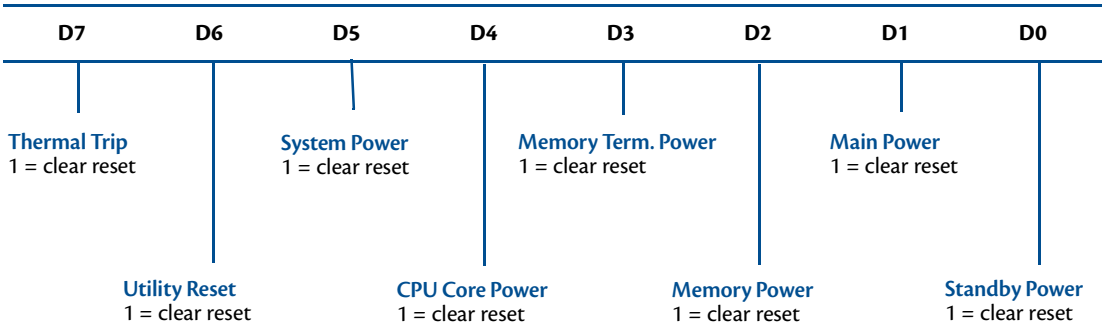


Table 51 Reset Status Description and Priorities

I/O Address EA8h	Reset Signal	Reset Priority[1]	Description
D7	Thermal Trip	2	Indicates that temperature has reached or exceeded the thermal trip limit. Its assertion will cause the system to trasition to S5 immediately. For more information, refer to *Hardware-Enforced Thermal Protection* on page 66.
D6	Utility Reset	—[2]	Utility connector push button reset[2]
D5	System Power	7	Power supplies that are not for standby power
D4	CPU Core Power	6	Power to the AMD G-Series FT1 CPU
D3	Memory Termination Power	5	Power to onboard memory termination
D2	Memory Power	4	Power to onboard memory banks
D1	Main Power	3	Main input power to cpuModule (+5V, +12V)
D0	Standby Power	1	Standby power supplies

1. When a reset is asserted, all resets with a higher reset priority will also be asserted. For example, if the standby power reset is asserted, all other resets will also be asserted.
2. The BIOS allows the user to change the function of the utility connector's push button reset, which thereby changes the power domain it controls (and its reset priority). Even if the push button is not configured as a reset, this bit will always read a 1 (asserted) when the reset button has been pushed.

Features and Settings That Can Affect Boot Time

The boot time of a system is dependent upon numerous system settings as well as devices attached to a system. This section addresses some devices and settings that can increase or decrease a system's boot time.

Boot Device Order

The BIOS contains a list of devices to try booting from. If you wish to boot to a particular device (for example, a hard drive), make sure that it is first in the boot order. This will speed up boot times.

Add-On Cards With BIOS Extensions

Some add-on cards have an integrated BIOS extension. The most common examples are SCSI controllers and network cards with boot ROMs. During POST, the BIOS executes the card's extension code. This extension code is third-party code, which is beyond RTD's control. The BIOS extension will most likely increase the boot time. Exactly how much it increases boot time will depend on the particular card and firmware version.

VGA Controller

VGA controllers have a VGA BIOS that must be initialized during POST. It can take some time to initialize the VGA BIOS. Exactly how long will depend on the particular VGA controller and BIOS version.

Hard Drive Type

During Hard Drive initialization, each device must be probed. Some devices take longer to probe. 2.5-inch hard drives tend to take longer than 3.5-inch ones, because they spin at a lower RPM.

Monitor Type

Some monitors take a while to power on. Desktop flat panels are especially slow. This does not affect the actual boot time of the CPU. However, the CPU may boot before the monitor powers on.

Network (PXE) Boot

The Ethernet controllers on the CMX34GS support Preboot Execution Environment (PXE) which permits the cpuModule to boot using a network interface. The PXE Boot ROM, which allows booting over the network, may be disabled in the BIOS to speed up boot time.

System Recovery

Reset Button Recovery

The CMX34GS provides several methods for recovering from an incorrectly configured system. In order to enter the recovery mode, follow the steps below:

1. Remove power from the system, including standby power.
2. Press and hold the reset button attached to the Utility Port 2.0 connector.
3. Apply power to the system while continuing to hold the reset button.
4. Wait the amount of time shown in Table 52 for the desired recovery mode.
5. Release the reset button, allowing the system to boot.

Table 52 Reset Button Recovery Modes

Hold Time[1]	Mode
0-4 seconds	No recovery mode. System will stay in reset while button is pressed.
4-8 seconds	Reserved
8-12 seconds	Serial POST Code Output

1. To assist with timing while the reset button is pushed, the LED will blink OFF at 5 second intervals.

Load Default BIOS Settings

Loading BIOS defaults allows recovery from an incorrectly configured display device, incorrect boot options, and many other incorrect settings. It is also a good starting point when making BIOS changes. After restoring defaults, the BIOS settings should be reviewed and modified as needed.

The default BIOS can be restored by the “Load RTD Defaults” option in the BIOS.

Serial Power-On-Self-Test (POST) Code Output

The POST Codes represent a series of events that take place in a system during the Power On Self Test. If the POST fails, the system will not boot as expected. Knowing which POST code the failure occurred may help system debug.

This recovery mode configures serial port connector **CN7** as single RS-232, and sends the POST codes on the transmit pin. The port settings are 115kbps, 8 bits, no parity, one stop bit. When using this recovery mode, the POST codes can be logged on another computer running terminal software. Contact RTD technical support for more details.

Note *POST Codes over the serial port (**CN7**) may also be enabled by installing **JP5** and **JP6** prior to power cycling the cpuModule. For more information, see Jumper Settings and Locations on page 76.*

Appendix A Hardware Reference

This appendix provides information on CMX34GS cpuModule hardware, including:

Jumper Settings and Locations — page 76

Onboard PCI/PCIe Devices — page 77

Physical Dimensions — page 78

Jumper Settings and Locations

Many cpuModule options are configured by positioning jumpers. Jumpers are labeled on the board as **JP** followed by a number.

Figure 7 shows the jumper locations that are used to configure the cpuModule. Table 53 lists the jumpers and their settings.

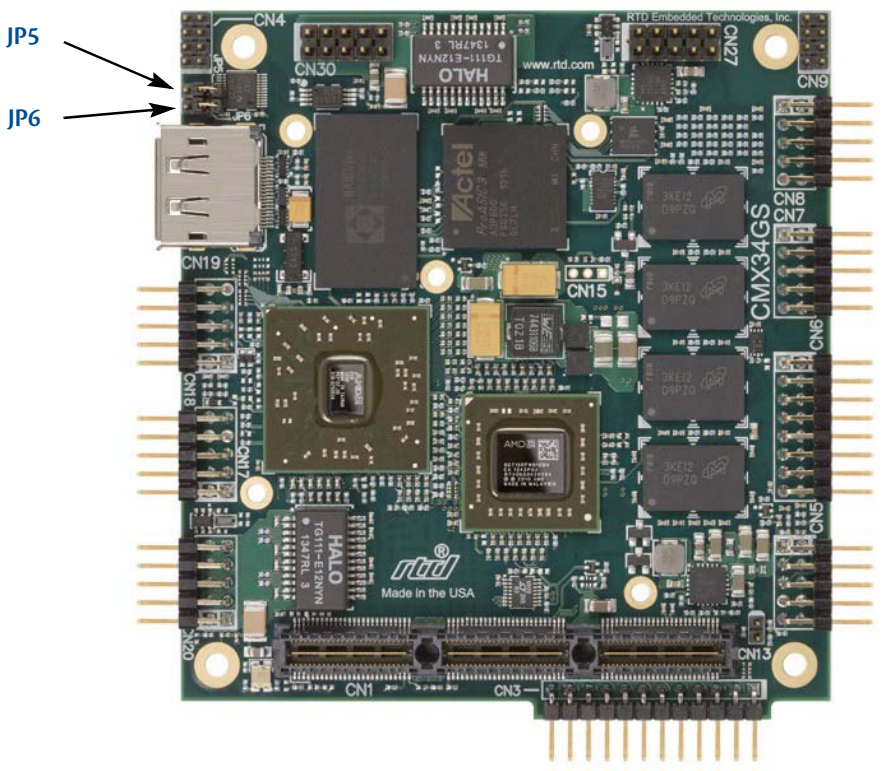


Figure 7 CMX34GS Jumper Locations (top side)

Table 53 CMX34GS Jumpers

Jumper	Pins	Function	Default
JP5	2	Reserved	open
JP6	2	Used to disable the Bus Stacking Error detection. See *PCIe/104 Type 2 Compatibility* on page 47. **pins 1–2**: Disable Bus Stacking Error detection **open**: Enable Bus Stacking Error detection (normal operation)	open
JP5 + JP6	2	Used to configure serial port connector **CN7** as single RS-232, and sends the POST codes on the transmit pin. See *Serial Power-On-Self-Test (POST) Code Output* on page 73 **pins 1–2 (JP5 and JP6)**: Enable POST Codes over Serial Port **CN7** **open**: Normal operation	open

Onboard PCI/PCIe Devices

The CMX34GS cpuModule has several onboard PCI/PCIe devices, all of which are listed in the table below. This table shows a typical configuration, and the actual devices may change based on BIOS settings.

Table 54 Onboard PCI Devices

Device ID	Vendor ID	Description
1510	1022	Host bridge
9804 / 9807 [1]	1002	VGA-compatible controlle
1314	1002	HD Audio controller
4390	1002	IDE controller (**CN1** & **CN2** PCIe/104 SATA links)
4397	1002	Univsersal Serial Bus (USB) OHCI
4396	1002	Univsersal Serial Bus (USB) EHCI
4397	1002	Univsersal Serial Bus (USB) OHCI
4396	1002	Univsersal Serial Bus (USB) EHCI
4385	1002	SMBus (System Management Bus)
439C	1002	IDE controller (onboard SATA storage)
439D	1002	ISA bridge
4384	1002	PCI-to-PCI bridge
43A0	1002	PCI-to-PCI bridge
43A3	1002	PCI-to-PCI bridge
1700	1022	Host bridge
1701	1022	Host bridge
1702	1022	Host bridge
1703	1022	Host bridge
1704	1022	Host bridge
1718	1022	Host bridge
1716	1022	Host bridge
1719	1022	Host bridge
10D3	8086	Ethernet Controller (**CN20**)
10D3	8086	Ethernet Controller (**CN30**)

1.The device ID for the VGA-compatible controller is 9804 for 615 MHz single-core models, and 9807 for 1.0 GHz dual-core models

Physical Dimensions

Figure 8 shows the mechanical dimensions of the CMX34GS cpuModule.

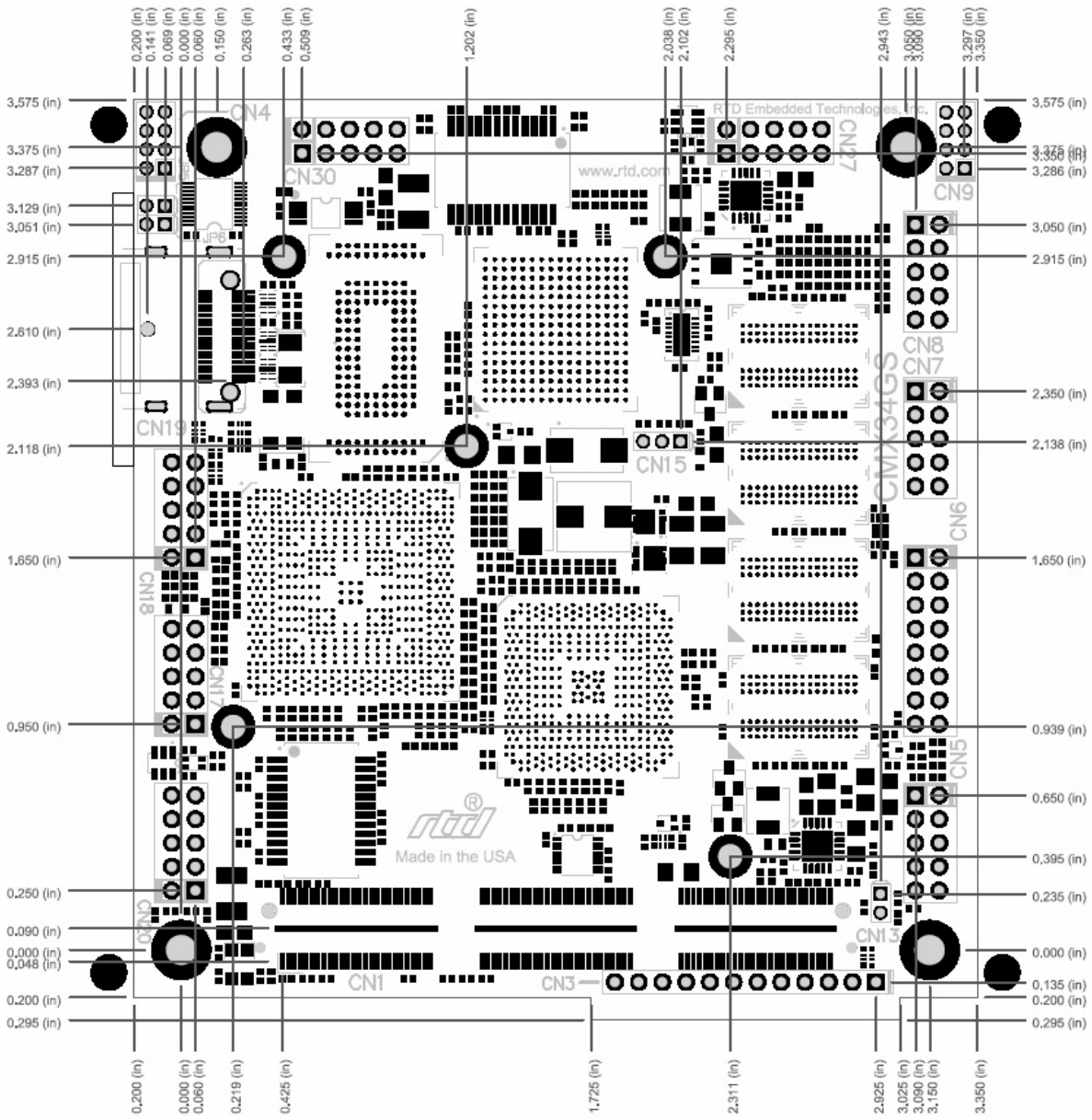


Figure 8 CMX34GS Physical Dimensions (±0.005 inches)

Appendix B Troubleshooting

Many problems you may encounter with operation of your CMX34GS cpuModule are due to common errors. This appendix includes the following sections to help you get your system operating properly.

Common Problems and Solutions — page 80

Troubleshooting a PC/104 System — page 81

How to Obtain Technical Support — page 82

Common Problems and Solutions

Table 55 lists some of the common problems you may encounter while using your CMX34GS cpuModule, and suggests possible solutions.

If you are having problems with your cpuModule, review this table before contacting RTD Technical Support.

Table 55 Troubleshooting

Problem	Additional Symptoms	Possible Cause(s)
cpuModule does not boot (no video output)	LED is red (in reset)	Input power is inadequate. Refer to Chapter 1, *Electrical Characteristics*. Verify input voltages are correct. If power is supplied via **CN3**, check for cabling issues.
		Malfunctioning peripheral card. Remove all peripheral cards from the system.
	LED is yellow (in standby)	cpuModule is in "Soft Off" due to operating system shutdown. Press power button to wake.
		ATX power supply is not turning on. Check jumpers on power supply. Verify PSON# signal.
	LED is cyan (bus stacking error)	See Chapter 3, *PCIe/104 Type 2 Compatibility*
	LED is green (normal operation)	cpuModule may be booted, but video is not connected properly. Attach a keyboard and verify the operation of the Num Lock and Caps Lock LEDs. If they respond as expected, the cpuModule is booted. Check the video cable connections.
		Video output may have been disabled in the BIOS. Try loading BIOS defaults per Chapter 4, *System Recovery*.
		If a PCI device is installed, the slot selection switch/jumpers may not be set correctly.
		Peripheral card may be interfering with boot sequence. Remove all peripheral cards from the system.
cpuModule reboots unexpectedly	cpuModule is running Windows	By default, Windows will automatically reboot when a Bugcheck (Blue Screen) is triggered. Disable this feature in the Control Panel. This will allow you to see the error and identify the root cause.
	cpuModule is powered via Auxiliary Power Connector (**CN3**)	Power cabling issues. Verify all pins on **CN3** are reliably connected with proper gauge wires.
		Power supply noise or current limiting. Check power pins with an oscilloscope and verify they remain in range.
		Power supply may not respond quickly enough to changes in power consumption. Switch to a different power supply (a PCI Express power supply is recommended)
	Peripheral card(s) installed	Peripheral card(s) may be overloading the power supply. Reduce the system to just the cpuModule and power supply and see if the problem re-appears. (Note that **CN3** is intended for powering the cpuModule only.)
cpuModule does not boot to USB device	USB device has a high power draw (e.g. DVD or hard drive)	Some USB devices are not fully compliant and draw too much current. Consider switching to a self-powered USB device with its own AC/DC power supply.
Date/time not saved when system is off	No RTC battery	A battery must be attached to the Utility Port 2.0 connector (**CN5**) to maintain date/time when main power is removed. For a list of alternate battery inputs, refer to *Real Time Clock Control* — page 62.
System performance lower than expected	LED is white	cpuModule is overheating and the processor is throttling. Increase the cooling (more airflow, larger heatsink, etc).

Troubleshooting a PC/104 System

If you have reviewed the preceding table and still cannot isolate the problem with your CMX34GS cpuModule, please try the following troubleshooting steps. Even if the resulting information does not help you find the problem, it will be very helpful if you need to contact technical support.

1. **Simplify the system**. Remove items one at a time and see if one particular item seems to cause the problem.
2. **Swap components**. Try replacing items in the system one-at-a-time with similar items.

How to Obtain Technical Support

If after following the above steps, you still cannot resolve a problem with your CMX34GS cpuModule, please gather the following information:

- cpuModule model, BIOS version, and serial number
- List of all boards in system
- List of settings from cpuModule Setup program
- Printout of autoexec.bat and config.sys files (if applicable)
- Description of problem
- Circumstances under which problem occurs

Then contact RTD Technical Support:

Phone: 814-234-8087

Fax: 814-234-5218

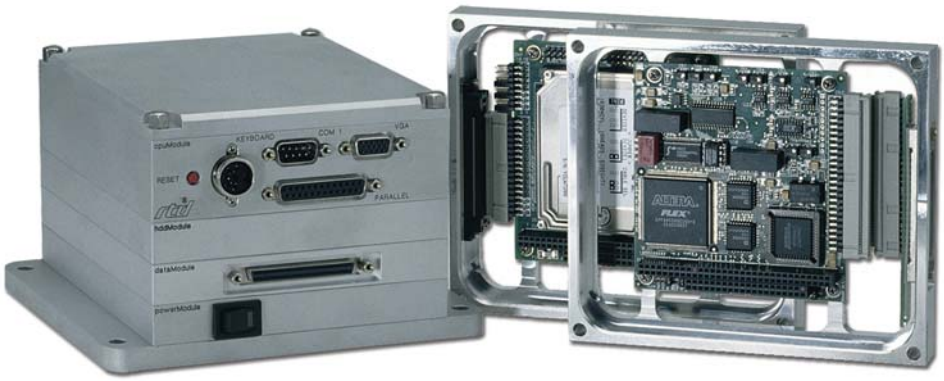
E-mail: techsupport@rtd.com

Appendix C IDAN™ Dimensions and Pinout

Like all other RTD PC/PCI-104 and PCIe/104 modules, cpuModules can be packaged in Intelligent Data Acquisition Node (IDAN) frames, which are milled aluminum frames with integrated heat sinks and heat pipes for fanless operation. RTD modules installed in IDAN frames are called building blocks. IDAN building blocks maintain the simple but rugged stacking concept of PC/PCI-104 and PCIe/104. Each RTD module is mounted in its own IDAN frame and all I/O connections are brought to the walls of each frame using standard PC connectors.

On the CMX34GS, no connections are made from module to module internal to the system other than through the PCIe/104 Type 2 bus, enabling quick interchangeability and system expansion without hours of rewiring and board redesign.

The CMX34GS cpuModule can also be purchased as part of a custom-built RTD HiDAN™ or HiDAN*plus*™ High Reliability Intelligent Data Acquisition Node. This appendix provides the dimensions and pinouts of the CMX34GS installed in an IDAN frame. Contact RTD for more information on high reliability IDAN, HiDAN, and HiDAN*plus* PC/PCI-104 systems.



IDAN—Adhering to the PC/PCI-104 and PCIe/104 stacking concept, IDAN allows you to build a customized system with any combination of RTD modules.

IDAN Heat Pipes—Advanced heat pipe technology maximizes heat transfer to heat sink fins.

HiDAN*plus*—Integrating the modularity of IDAN with the ruggedization of HiDAN, HiDAN*plus* enables connectors on all system frames, with signals running between frames through a dedicated stack-through raceway.

IDAN Dimensions and Connectors

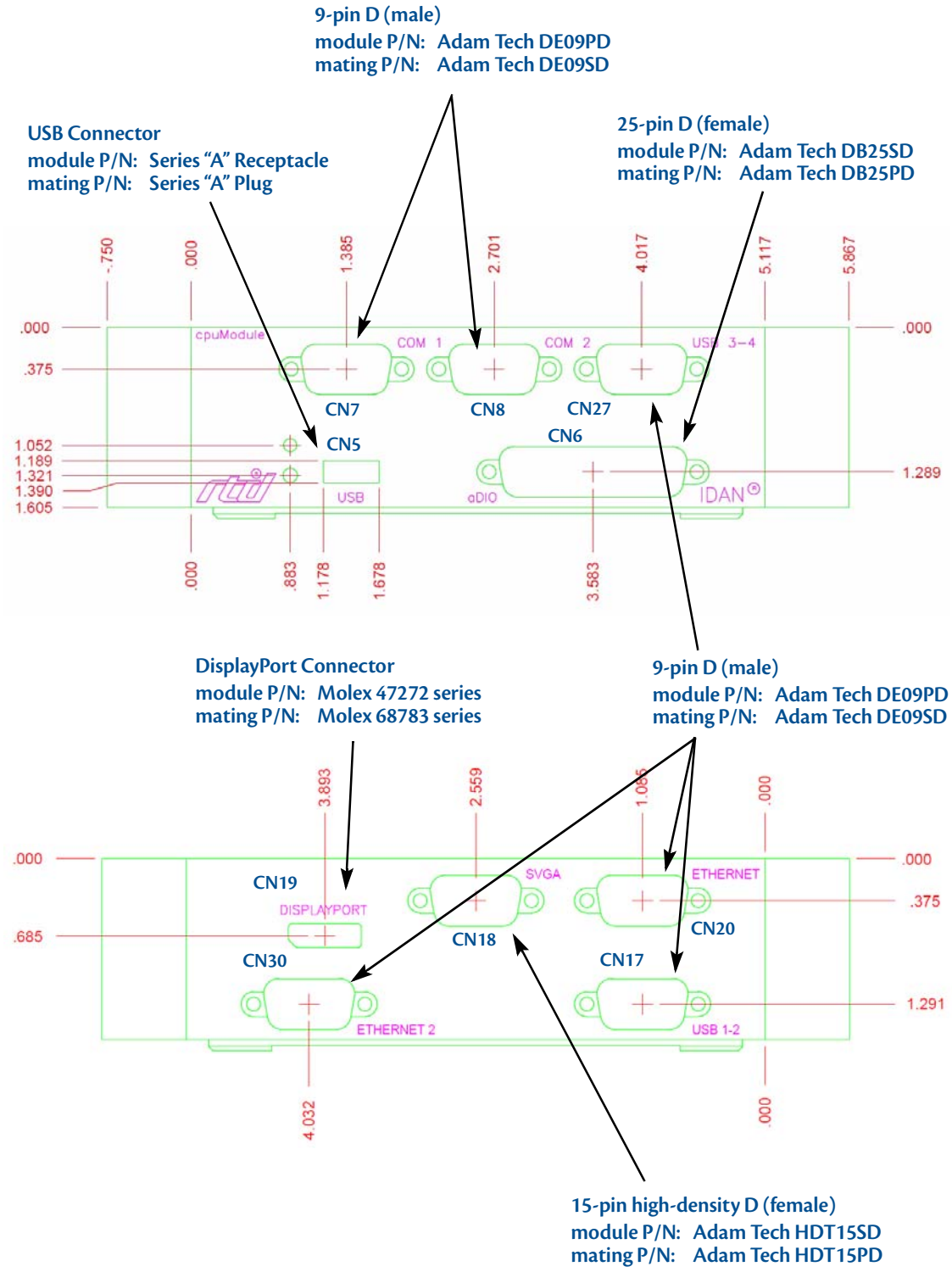


Figure 9 IDAN-CMX34GS Connectors[1]

1. Use 40mm for this frame when calculating bolt lengths.

IDAN Contents

The IDAN-CMX34GS contains both a CMX34GS cpuModule and a SATA34106 carrier for a 2.5" SATA drive. Also inside the IDAN-CMX34GS unit is a CMOS battery which is connected to the battery input connection of the cpuModule's Utility Port 2.0 connector. The frame of the IDAN-CMX34GS brings out the cpuModule's multi-color LED as well as the cpuModule's reset button. (The cpuModule's power button is not accessible from the exterior of the frame, but the reset button is configurable as as a power button through the BIOS.)

For more information on cpuModule's battery input and reset button input on the Utility Port 2.0 connector, refer to the *Utility Port 2.0 Connector (CN5)* on page 29.

External I/O Connections

Table 56 COM1/COM2 (Single Port Mode)— 9-Pin D Connector (male)

CPU Pin	IDAN Pin (DB-9)	Single RS-232	Single RS-422	Single RS-485
1	1	DCD	TXD–	D–
2	6	DSR	—	—
3	2	RXD	TXD+	D+
4	7	RTS	—	—
5	3	TXD	RXD+	—
6	8	CTS	—	—
7	4	DTR	RXD–	—
8	9	RI	—	—
9,10	5	GND	GND	GND

Table 57 COM1/COM2 (Dual Port Mode)— 9-Pin D Connector (male)

CPU Pin	IDAN Pin (DB-9)	Dual RS-232	Dual RS-422	Dual RS-485
1	1	DCD1	TXD1-	D1-
3	2	RXD1	TXD1+	D1+
5	3	TXD1	RXD1+	—
7	4	DTR1	RXD1-	—
9,10	5	GND	GND	GND
2	6	DSR1	TXD2-	D2-
4	7	TXD2	TXD2+	D2+
6	8	RXD2	RXD2+	—
8	9	RI1	RXD2-	—

Table 58 aDIO — 25-Pin D Connector (female)

IDAN Pin #	aDIO Port	CPU Pin #
1	P0-0	1
2	P0-2	3
3	P0-4	5
4	P0-6	7
5	Strobe 0	9
6	P1-0	11
7	P1-2	13
8	GND	15
9	reserved	-

Table 58 aDIO — 25-Pin D Connector (female)

IDAN Pin #	aDIO Port	CPU Pin #
10	reserved	-
11	reserved	-
12	reserved	-
13	reserved	-
14	P0-1	2
15	P0-3	4
16	P0-5	6
17	P0-7	8
18	Strobe 1	10
19	P1-1	12
20	P1-3	14
21	+5 V	16
22	reserved	-
23	reserved	-
24	reserved	-
25	reserved	-

Table 59 SVGA — 15-Pin High Density D Connector (female)

IDAN Pin #	Signal	Function	CPU Pin #
1	Red	Red Analog Output	4
2	Green	Green Analog Output	6
3	Blue	Blue Analog Output	8
4	Reserved	Reserved	—
5	GND	Ground	9
6	GND	Ground	9
7	GND	Ground	9
8	GND	Ground	10
9	+5 V	+ 5 Volts	7
10	GND	Ground	10
11	Reserved	Reserved	—
12	DDC Data	Monitor data	5
13	HSYNC	Horizontal Sync	2
14	VSYNC	Vertical Sync	1
15	DDC CLK	Monitor Clock	3

Table 60 DisplayPort Connector

Pin	Signal	Standard Function	Dual-mode (DP++) Function (DVI / HDMI mode)[1]	In/Out
1	LN0+	Main Link, Lane 0 (positive)	TMDS Channel 2 (positive)	out
2	GND	Ground	Ground	out
3	LN0-	Main Link, Lane 0 (negative)	TMDS Channel 2 (negative)	out
4	LN1+	Main Link, Lane 1 (positive)	TMDS Channel 1 (positive)	out
5	GND	Ground	Ground	out
6	LN1-	Main Link, Lane 1 (negative)	TMDS Channel 1 (negative)	out
7	LN2+	Main Link, Lane 2 (positive)	TMDS Channel 0 (positive)	out
8	GND	Ground	Ground	out
9	LN2-	Main Link, Lane 2 (negative)	TMDS Channel 0 (negative)	out
10	LN3+	Main Link, Lane 3 (positive)	TMDS Clock (positive)	out
11	GND	Ground	Ground	out
12	LN3-	Main Link, Lane 3 (negative)	TMDS Clock (negative)	out
13	CFG1	Configuration Pin 1	Cable Adapter Detect	out
14	CFG2	Configuration Pin 2	Consumer Electronics Control[2]	out
15	AUX+	Auxiliary Channel (positive)	DDC Clock	in/out
16	GND	Ground	Ground	out
17	AUX-	Auxiliary Channel (negative)	DDC Data	in/out
18	HPD	Hot Plug Detect	Hot Plug Detect	in
19	DPG	Return for DPV	Return for DPV	out
20	DPV	+3.3V DC Power	+3.3V DC Power	out

1.Requires special passive adapter
2.HDMI mode only

Facing DisplayPort connector, the pinout is:

19	17	15	13	11	9	7	5	3	1
DPG	AUX-	AUX+	CFG1	GND	LN2-	LN2+	GND	LN0-	LN0+
DPV	HPD	GND	CFG2	LN3-	LN3+	GND	LN1-	LN1+	GND
20	18	16	14	12	10	8	6	4	2

Table 61 USB — 9-Pin D Connector (male)

IDAN Pin #	Signal	Function	Mode
1	VCC1	+5 V to USB1	output
2	Data USB1–	USB1 Data–	input/output
3	Data USB1+	USB1 Data+	input/output
4	GND	Ground	—
5	GND	Ground	—
6	VCC2	+5 V to USB2	output
7	Data USB2–	USB2 Data–	input/output
8	Data USB2+	USB2 Data+	input/output
9	GND	Ground	—

Table 62 Ethernet — 9-Pin D Connector (female)

IDAN Pin #	RJ-45 Pin	Signal	CPU Pin #
1	3	B+ (RX+)	1
2	4	C+	3
3	1	A+ (TX+)	5
4	7	D+	7
5	—	Ground	9
6	6	B- (RX–)	2
7	5	C-	4
8	2	A- (TX–)	6
9	8	D-	8

Appendix D Additional Information

Application Notes

RTD offers many application notes that provide assistance with the unique feature set of the CMX34GS cpuModule. For the latest application notes, refer to the RTD website.

Drivers and Example Programs

To obtain the latest versions of drivers and example programs for this cpuModule, refer to the RTD website.

Interrupt Programming

For more information about interrupts and writing interrupt service routines, refer to the following book:

Interrupt-Driven PC System Design
by Joseph McGivern
ISBN: 0929392507

Serial Port Programming

For more information about programming serial port UARTs, consult the following book:

Serial Communications Developer's Guide
by Mark Nielson
ISBN: 0764545701

PC/104 Specifications

A copy of the latest PC/104specifications can be found on the webpage for the PC/104 Embedded Consortium:

http://www.pc104.org

Appendix E Limited Warranty

RTD Embedded Technologies, Inc. warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from RTD Embedded Technologies, Inc. This warranty is limited to the original purchaser of product and is not transferable.

During the one year warranty period, RTD Embedded Technologies will repair or replace, at its option, any defective products or parts at no additional charge, provided that the product is returned, shipping prepaid, to RTD Embedded Technologies. All replaced parts and products become the property of RTD Embedded Technologies. Before returning any product for repair, customers are required to contact the factory for a Return Material Authorization number.

This limited warranty does not extend to any products which have been damaged as a result of accident, misuse, abuse (such as: use of incorrect input voltages, improper or insufficient ventilation, failure to follow the operating instructions that are provided by RTD Embedded Technologies, “acts of god” or other contingencies beyond the control of RTD Embedded Technologies), or as a result of service or modification by anyone other than RTD Embedded Technologies. Except as expressly set forth above, no other warranties are expressed or implied, including, but not limited to, any implied warranties of merchantability and fitness for a particular purpose, and RTD Embedded Technologies expressly disclaims all warranties not stated herein. All implied warranties, including implied warranties for merchantability and fitness for a particular purpose, are limited to the duration of this warranty. In the event the product is not free from defects as warranted above, the purchaser's sole remedy shall be repair or replacement as provided above. Under no circumstances will RTD Embedded Technologies be liable to the purchaser or any user for any damages, including any incidental or consequential damages, expenses, lost profits, lost savings, or other damages arising out of the use or inability to use the product.

Some states do not allow the exclusion or limitation of incidental or consequential damages for consumer products, and some states do not allow limitations on how long an implied warranty lasts, so the above limitations or exclusions may not apply to you.

This warranty gives you specific legal rights, and you may also have other rights which vary from state to state.

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